Low-Temperature Atomic Layer Deposition of Hafnium Oxide Gate Dielectrics

Bachelor Thesis

Benjamin Roth

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Supervisors:

Prof. Dr. Erwann Bocquillon

Torsten Röper

Second Examiner:

Prof. Dr. Markus Grüninger

Institute of Physics II

Faculty of Mathematics and Natural Sciences

University of Cologne

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Abstract

The quantum anomalous Hall effect (QAHE), first experimentally observed in 2013 [1], is a fascinating quantum phenomenon that continues to be a focus of active research. The QAHE is characterized by a single chiral edge state. To suppress bulk transport, the Fermi level is tuned in the bulk's band gap by electrostatic gating. However, the deposition of gate material often requires elevated temperatures, at which our samples degrade. Hence, we develop and optimize the low-temperature ($< 100\,^\circ\mathrm{C}$) atomic layer deposition of hafnium oxide (HfO_2) gate dielectrics. We found relative permittivities ϵ_r of 6 to 10, which were significantly lower than in other studies. Current-voltage measurements showed strong asymmetry, with electrical breakdowns occurring at $E_\mathrm{bd} \sim 1.5\,\mathrm{MV\,cm^{-1}}$ and up to $E_\mathrm{bd} \sim 6\,\mathrm{MV\,cm^{-1}}$ depending on the voltage polarity. Finally, we deposited HfO_2 at $80\,^\circ\mathrm{C}$ on a quantum anomalous Hall insulator (QAHI), where a successful gating effect was shown at $T \approx 14\,\mathrm{mK}$. These results highlight the potential for atomic layer deposition of hafnium oxide for temperature-sensitive gating applications.

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1. Introduction

The quantum anomalous Hall effect (QAHE) was discovered in 2013 and is a fascinating quantum phenomenon. It is characterized by a single dissipationless edge channel, giving rise to a quantized Hall conductance in the absence of magnetic fields [1–4]. It remains a topic of ongoing research due to its potential applications in quantum computing and low-power electronics. However, electrostatic gating is beneficial for observing the QAHE by suppressing bulk transport.

Electrostatic gating is an important tool for manipulating the behavior of microelectronic devices, by controlling the charge carrier density. Gating is realized by depositing a thin insulating film (gate dielectric) and a conducting layer (gate electrode) on top of the device. This arrangement resembles a plate capacitor. By applying a voltage to the gate electrode, positive and negative charge carriers accumulate in the gate electrode and the sample itself respectively. This effectively changes the Fermi level in the gated system. To maximize the gate effect, a gate dielectric with high relative permittivity, high electric breakdown field, and low leakage current is needed. However, the quantum anomalous Hall insulator (QAHI) degrades at elevated temperatures, which are common during gate material deposition. Hence, we need to develop a deposition process capable of depositing below $\sim$100 °C. Within those constraints, hafnium oxide (HfO_2) emerges as a promising gate dielectric, possessing all crucial properties. The deposition technique used in this work is atomic layer deposition (ALD), enabling atomic-scale thickness controllability, reproducibility, and layer conformality due to its self-limiting nature. In addition, the ALD process does not intrinsically rely on high deposition temperatures. This leads to the topic of this thesis, which is the optimization of the deposition process of hafnium oxide at low temperatures (< 100 °C) to be used on thermally sensitive devices.

This thesis is organized into five chapters. Chapter 2 establishes a theoretical background on the QAHE and electrostatic gating. In Chapter 3 the ALD process and setup, as well as the effect of important deposition parameters are discussed and experimentally studied. Chapter 4 deals with the electrical characterization of the HfO_2 films. This includes the fabrication of test devices, capacitance measurements, and current-voltage measurements, to assess the permittivity and breakdown field. Lastly, in Chapter 5, the deposition process is used on a QAHE sample, where a gating effect is demonstrated.

2. Quantum Hall effects and the role of gates

2.1 Classical Hall effect

The classical Hall effect is a phenomenon, in which a voltage emerges perpendicular to the current direction. This effect occurs when a current-carrying strip is subject to an out-of-plane magnetic field. In this setup, a voltage perpendicular to both the current and the magnetic field evolves across the strip, called the *Hall voltage*. This can be explained with the classical equations of motion for charged particles in a magnetic field, specifically the *Lorentz force* (Eq. 2.1), which demonstrates, that moving charged particles are deflected perpendicular to their velocity [5, 6].

$$\vec{F} = q\left(\vec{E} + \vec{v} \times \vec{B}\right) \tag{2.1}$$

The resulting imbalance in the charge carrier density on either side of the current-carrying strip gives rise to an electric field that counteracts further accumulation of charges [5, 6]. To facilitate the calculations and prepare for the quantum Hall effect (typically observed in two-dimensional samples [6, 7]), the current-carrying strip is assumed to be infinitely thin in its z direction, constraining the particle's motion to the xy-plane. The current is flowing in the x direction, while the magnetic field acts in the z direction. The Hall voltage will then evolve across the y direction. This enables us to describe the charge transport with two-dimensional coordinates, leading to the following equations [7, 8].

$$\mathbf{E} = \rho\,\mathbf{J} \tag{2.2}$$

$$\rho = \frac{m}{ne^2\tau}\begin{pmatrix} 1 & \omega_B\tau \\ -\omega_B\tau & 1 \end{pmatrix} \tag{2.3}$$

With the cyclotron frequency $\omega_B = \frac{eB}{m}$, the mean time between scattering events τ, the charge carrier density n, the current density $\mathbf{J}$ and the electric field $\mathbf{E}$. A force $-m\mathbf{v}/\tau$ was added in addition to the Lorentz force, which represents the scattering of charges. Without a magnetic field, the off-diagonal components of the resistivity tensor ρ vanish, reducing Eq. 2.3 to just the simple relation $E_i = \rho J_i$, analogous to Ohm's law $U = RI$. The longitudinal resistivity $\rho_{xx} = \frac{m}{ne^2\tau}$ is, as expected, dependent on the scattering time, and therefore the sample temperature and/or purity, but is independent of the magnetic field. The transverse resistivity $\rho_{xy} = \frac{B}{ne}$ on the other hand, is independent of the scattering time, which makes it promising for the investigation of properties like the charge carrier density with very high precision. Furthermore, it depends linearly on the magnetic field B [7, 8].

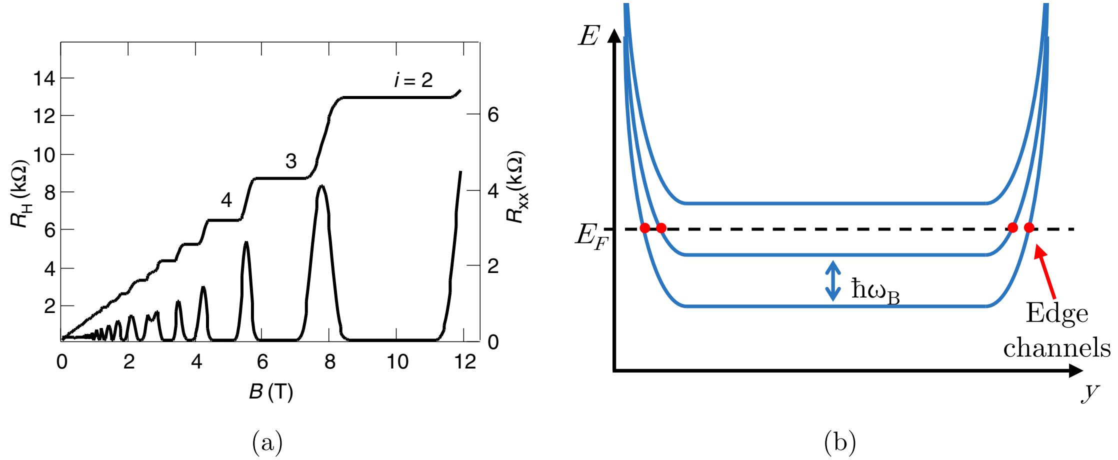
2.2 Quantum Hall effect

The quantum Hall effect is the quantum limit of the classical Hall effect, in which the transverse resistivity ρ_{xy} takes on quantized values. It can be observed in two-dimensional electron gases (2DEGs) at low temperatures and very strong magnetic fields [6–8]. From the classical Hall effect, the dependence of ρ_{xx} and ρ_{xy} on the magnetic field is predicted to be constant for ρ_{xx} and linearly increasing for ρ_{xy} (Eq. 2.3). In contrast to this classical prediction, ρ_{xy} takes on quantized values and stays exactly at those values over a range of magnetic fields, as shown in Fig. 2.1 (a) [7–10].

$$\rho_{xy} = \frac{h}{e^2}\frac{1}{\nu} \tag{2.4}$$

The actual values of ρ_{xy} are determined only by fundamental physical constants, and the *filling factor* ν, which takes on integer or fractional positive values. For $\nu = 1$, the value of $\rho_{xy} = h/e^2 = 25\,812.807\,45...\,\Omega = R_K$ is called the *von Klitzing constant* [9, 10].
These regimes of constant values of transverse resistivity are the so-called *Hall plateaus*. While the transverse resistivity is inside a Hall plateau, the longitudinal resistivity drops to zero and only spikes, when ρ_{xy} changes from one plateau to another [6, 7, 10]. The centers of these plateaus occur at magnetic field strengths of

$$B = \frac{n}{\nu}\Phi_0 \tag{2.5}$$



(a) (b)

Fig. 2.1: (a) Experimental measurements of the Hall resistance R_{H} and of the longitudinal resistance R_{xx} for a Si-MOSFET ($B = 13.8\,\mathrm{T}$) and a GaAs/AlGaAs heterostructure at a temperature of 0.3 K, taken from Jeckelmann and Jeanneret [11]. (b) Energy of the Landau levels as a function of position. The Fermi Energy (dashed line) lies between two levels inside the energy gap in the bulk. Edge channels (red dots) emerge at the edges, where the Fermi energy is crossed.

where $\Phi_0 = \frac{h}{e}$ is the magnetic *flux quantum*, a characteristic quantity of magnetic flux and n is the electron density in two dimensions [7, 10]. At a given magnetic field, the center of each plateau is therefore strongly influenced by the charge carrier density, which can be controlled by the *gate voltage* V_g [6].

The presence of plateaus can be explained as follows: The strong magnetic field gives rise to *Landau levels* which are the energy levels of charge carriers confined to circular orbits with the energy $E_n = \hbar\omega_B(n + \frac{1}{2})$, where ω_B is the cyclotron frequency [6–8, 12]. The energy differences between those levels are therefore $\hbar\omega_B$. With an increasing magnetic field, the energy of the Landau levels increases. At the edges of the sample, the Fermi level rises to the vacuum potential, manifesting as a steep rise in the Landau levels [9, 12]. The Landau levels are shown in Fig. 2.1 (b). At a given Fermi energy between two levels, the bulk of the sample is insulating, as the energy levels below are completely filled [6, 12]. Only at the edge, where Landau levels cross the Fermi energy, a one-dimensional transport channel arises [12]. The number of conducting channels is determined by the number of filled Landau levels, which correspond to the filling factor ν. In the edge

channels, no scattering can occur, explaining why the longitudinal resistance drops to zero [12]. The transverse resistance is determined by the number of conducting edge channels, each of which adds a conductance of e^2/h [9, 12]. Increasing the magnetic field leads to a decrease in filled Landau levels, corresponding to an increase in the transverse resistance until only the lowest Landau level is filled.

An interesting property of this effect is, that impurities or small defects in the bulk do not disturb the phenomenon, since the charge carriers are localized around those defects [9, 10, 12]. The conductance only occurs in the edge channels, where the energy of the Landau levels increases simultaneously around the whole sample [7, 9, 12].

2.3 Quantum anomalous Hall effect

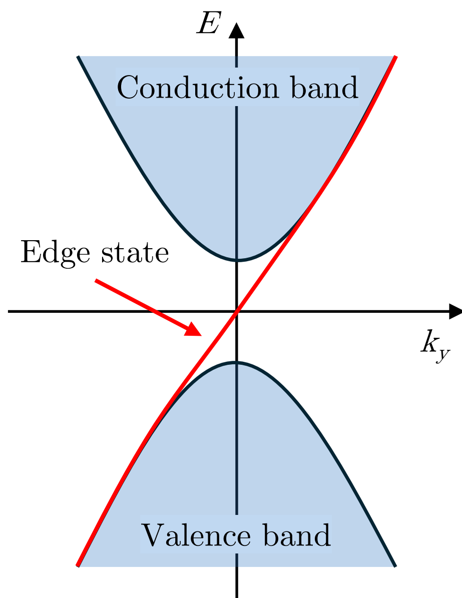


Fig. 2.2: Band structure of a quantum anomalous Hall insulator

The quantum anomalous Hall effect is similar to the quantum Hall effect, except that the quantization of the Hall resistance occurs due to the internal magnetization of the material rather than the application of an external magnetic field [13, 14]. In quantum anomalous Hall insulators (QAHI), this is characterized by a single gapless *edge state* which carries a current without dissipation, while the bulk of the material is insulating [14, 15]. Phenomenologically this is very similar to the quantum Hall effect in the $\nu = 1$ case.

To realize the quantum anomalous Hall effect we are using two-dimensional magnetic topological insulators. These are ferromagnetic materials that exhibit a topologically non-trivial band structure resulting in the conduction and valence bands crossing at the sample's surface as shown in Fig. 2.2 [15]. If the Fermi energy is inside the energy gap of the bulk, dissipationless edge states occur [13, 15]. Due to the topological nature of these edge states, they are protected against scattering on defects or impurities [13, 16]. To observe the quantum anomalous

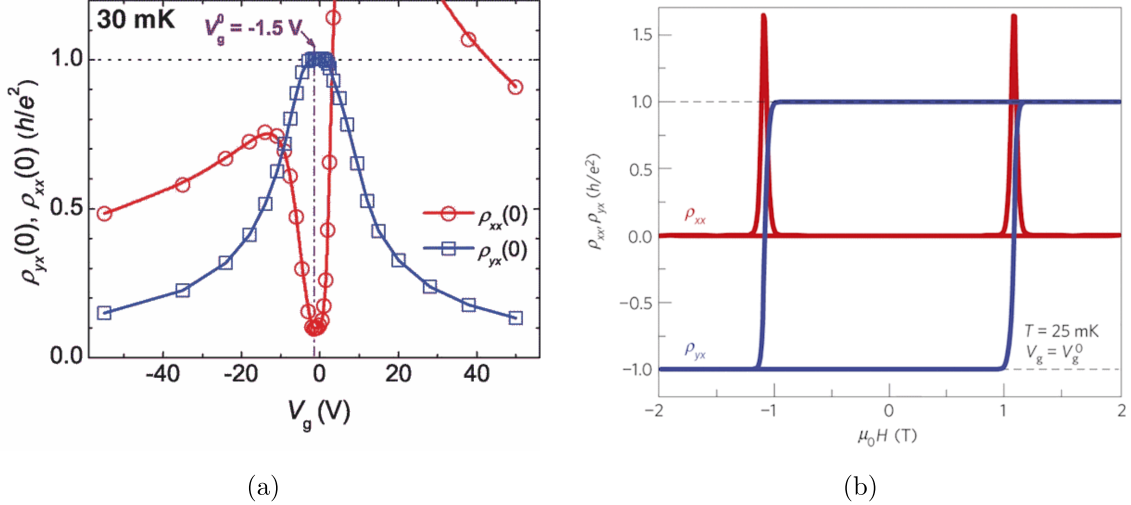


Fig. 2.3: (a) $\rho_{xy}(B = 0)$ and $\rho_{xx}(B = 0)$ as a function of gate voltage in thin films of chromium-doped $(Bi,Sb)_2Te_3$ at $T = 30\,\mathrm{mK}$; taken from Chang et al. [1]. (b) Magnetic field dependence of ρ_{xy} and ρ_{xx} in V-doped $(Bi,Sb)_2Te_3$ thin films measured at $T = 25\,\mathrm{mK}$ with V_g at V_g^0; taken from Chang et al. [2].

Hall effect in a QAHI, the Fermi level is tuned by applying a gate voltage. The dependence of the longitudinal and transverse resistance ρ_{xx} and ρ_{xy} on the gate voltage are shown in Fig. 2.3 (b). When the Fermi level is between the valence and conduction band of the material, as depicted in Fig. 2.2, the transverse resistance is quantized at h/e^2, while the longitudinal resistance goes to zero over a range of gate voltages [17]. After tuning the gate voltage, the magnetic field can be swept, to observe the behavior seen in Fig. 2.3 (a). Here the transverse resistance is quantized to h/e^2 even at zero magnetic field. The sign of the transverse resistance depends on the magnetization of the film, which changes its sign at the coercive field. [1, 14, 16, 17]

2.4 Electrostatic gating

In our work, the deposition of hafnium oxide (HfO_2) thin films as gate dielectrics on QAHIs is studied. In the quantum anomalous Hall effect, a gate is used to tune the charge carrier density and therefore the Fermi energy to lie within the band gap of the bulk to allow the formation of dissipationless edge channels [16, 17]. When working with

devices exhibiting the quantum anomalous Hall effect, a gate is fabricated on top or the back of the sample. The gate consists of a *gate electrode* separated from the device by an insulating layer, called the *gate dielectric*. Since oxides are the most common type of gate dielectrics, they are sometimes called *gate oxides*. This arrangement forms a capacitor between the sample and the gate. When a potential difference is applied, an electric field builds up across the gate dielectric and effectively changes the Fermi level inside the sample.

The dielectric layer, which is the topic of this thesis, has two critical properties. Firstly, the dielectric needs to be an effective insulator with a low leakage current, allowing for the application of large voltages before reaching electric breakdown. The breakdown voltage is the potential difference above which the dielectric becomes conductive. With a higher breakdown voltage, a greater range of charge carrier densities can be achieved. The breakdown voltage scales linearly with respect to the layer thickness d. Secondly, the gate dielectric must possess a high capacitance to significantly influence the charge carrier density within the sample. The capacitance of two parallel plates with area A and distance d between them is given by Eq. 2.6, where ϵ_0 is the permittivity of free space and ϵ_r is the relative permittivity of the gate dielectric.

$$C = \frac{\epsilon_0 \epsilon_\mathrm{r}}{d} A \tag{2.6}$$

High capacitance can be achieved by either decreasing the dielectric layer thickness d or by using a gate dielectric with a higher relative permittivity ϵ_r. Increasing the relative permittivity of the gate dielectric has the advantage of being able to use thicker dielectric layers, which in turn reduces leakage current and increases the breakdown voltage of the gate.

Having established the theoretical background necessary for understanding quantum anomalous Hall (QAH) measurements and explored the role and requirements of gating and gate materials, the next chapter will focus on the deposition of hafnium oxide as a gate dielectric.

3. Optimization of HfO_x deposition

To realize a gate effect in thermally sensitive devices, a deposition method capable of producing nanometer-scale insulator films at temperatures below ~100 °C is required. Given these constraints, atomic layer deposition (ALD) is a promising deposition technique. This chapter will cover both the theoretical aspects of precursor reactions and the working principles of atomic layer deposition (ALD), as well as an experimental comparison of various deposition parameters.

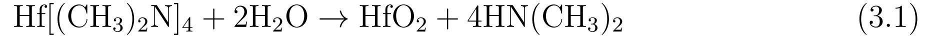
3.1 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a self-limiting deposition technique based on chemical reactions, in which the sample is exposed to each reactant sequentially. Because of the self-limiting nature of the process, the film thickness can be precisely controlled by the number of completed cycles, and a highly conformal and homogeneous film can be produced [18].

3.1.1 ALD setup

The machine used in this work is an *AT410* thermal ALD system by *Anric Technologies*. The reactants or *precursors* that are used to grow the hafnium oxide thin films are Tetrakis(dimethylamido)hafnium(IV) ($Hf[(CH_3)_2N]_4$, TDMAH) and water (H_2O). Although different types of precursor combinations can be used to grow hafnium oxide films, the combination of TDMAH and water was chosen, because of its high reactivity, which makes low-temperature deposition possible [19]. TDMAH is an organometallic compound consisting of a central hafnium atom that is weakly bound to four functional groups of

Dimethylamino ($(CH_3)_2N$ or NMe_2), which are called ligands [20]. Eq. 3.1 shows the chemical reaction of a single ALD cycle [19]:



$$Hf[(CH_3)_2N]_4 + 2H_2O \rightarrow HfO_2 + 4HN(CH_3)_2 \quad (3.1)$$

3.1.2 ALD process

The ALD cycle (when using two precursors) consists of four different steps, which are shown in Fig. 3.1. These reactions are simplified and may vary in the actual deposition. The simplified process steps are explained below.

1. **TDMAH pulse**
   The substrate is exposed to TDMAH, which reacts with the OH-Bonds present on the surface. The hydrogen atoms react with some of TDMAH's dimethylamino groups forming dimethylamine, while the hafnium binds to the oxygen atoms.

2. **N_2 purge**
   Dimethylamine and remaining TDMAH are removed by purging the reactor with Nitrogen, to avoid chemical reactions in the gas phase during the water pulse.

3. **H_2O pulse**
   The surface is exposed to water vapor which reacts with the remaining dimethylamino groups of the adsorbed TDMAH. Dimethylamine is formed, leaving behind OH-Bonds attached to the hafnium atoms.

4. **N_2 purge**
   In the last step of the cycle, the reactor is purged with nitrogen to remove dimethylamine and the residual water vapor.

Since the exact ratio of Oxygen and Hafnium in the deposited layers is unknown and can deviate from the ideal HfO_2 composition, as seen in [19, 21], the material is referred to as HfO_x in the following discussions, indicating that the O/Hf ratio may deviate from 2. Under ideal conditions, each step of the process is self-limiting. *Self-limiting* means that the reaction automatically terminates after interacting with the whole surface, resulting in the growth of a single layer per cycle. Growth per cycle may still be lower than one

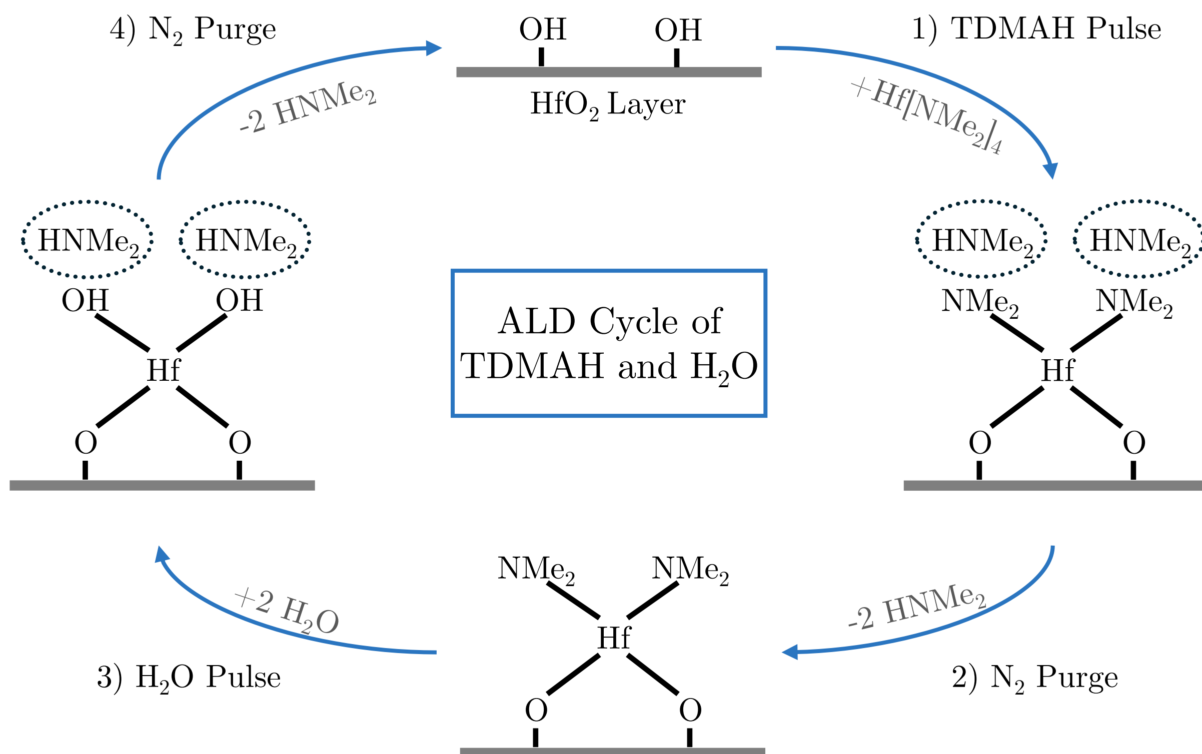


Fig. 3.1: Depicted are the four steps constituting an ALD cycle with TDMAH and H_2O: 1.) TDMAH Pulse, 2.) N_2 purge, 3.) H_2O pulse, 4.) N_2 purge. Me_2 is used as a short form for dimethyl $(CH_3)_2$. Chemical reactions are simplified from D'Acunto et al. [22].

lattice parameter because it is a statistical process that may not cover the entire surface in one cycle. In the precursor exposure steps, self-limiting behavior is reached after the whole surface is covered with the respective precursor. In the purging steps, the inert gas flushes all reaction byproducts out of the process chamber, after which the inert gas should not interact with the surface.

In reality, the reactions are only self-limiting if the growth conditions, like deposition and precursor temperature or the timing for each process step, are chosen appropriately. The influence of different growth parameters will be discussed in more detail in Sec. 3.1.3.

3.1.3 ALD windows and growth conditions

Various ALD parameters have a strong influence on the deposition quality. The most important parameter is the deposition temperature in the reaction chamber. Another im-

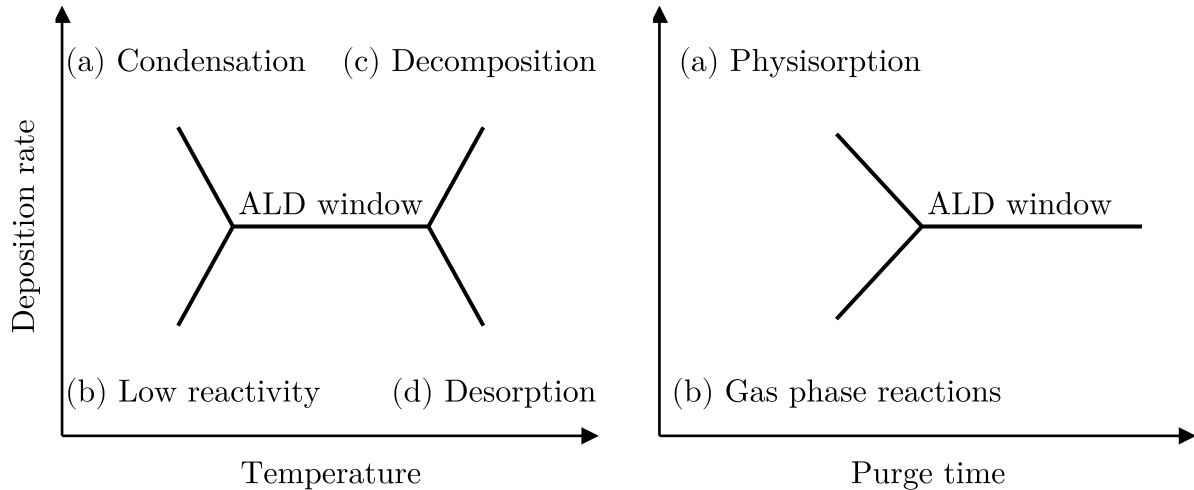


Fig. 3.2: ALD windows for deposition temperature (left) and purge times (right).

portant parameter, specifically at low deposition temperatures (<100 °C), is the precursor purge time [21]. These are the two parameters, which are varied in this work. Other parameters necessary for a successful ALD process, which were kept constant throughout all depositions, are among others precursor exposition times, purge gas flow rate, precursor temperatures, and process chamber pressure. These parameters are listed in Appendix A in Table A.1. The ALD cycle count was maintained at 300 cycles for all depositions.

For deposition temperature and purge times, there exist so-called *ALD windows* (Fig. 3.2), that describe a parameter range in which the deposition is self-limiting.

The deposition of materials at temperatures below the ALD window can result in either a high growth rate, which occurs due to the condensation of precursors, or a low growth rate, caused by the lack of sufficient thermal energy. At temperatures above the ALD window, material can desorb from the surface resulting in a lower growth rate. On the other hand, enhanced growth rates may occur at higher temperatures due to the decomposition of the precursor in the gas phase. This is the same mechanism used in chemical vapor deposition (CVD) [23]. The ALD window for purge times is different because there is no upper limit on the duration for which the process chamber can be purged, as shown in Fig. 3.2. If the purge time is too short, one precursor may not be fully removed and can subsequently react with the other precursor in the gas phase instead of on the surface. If the HfO_x adheres to the surface due to physical interaction, called physisorption,

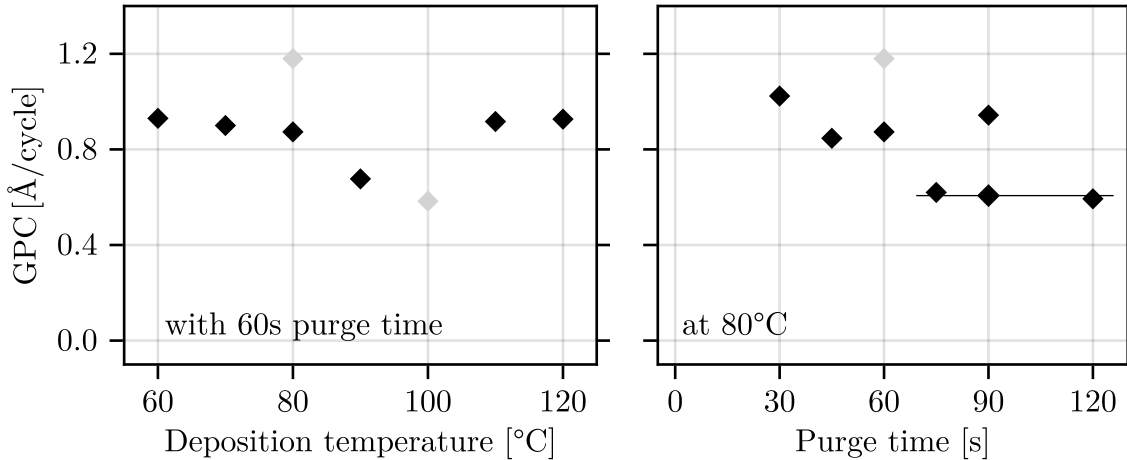


Fig. 3.3: HfOx growth rate as a function of (left) deposition temperature for 60 s purge times (right) purge time at 80 °C deposition temperature. Light gray data represents the first two samples grown and is therefore considered unreliable.

enhanced growth rates may occur. If it is instead removed during the purging step, lower than expected growth rates are observed [23]. At low-temperature depositions, such as ours, sufficiently long purge times are particularly important, as shown by Shekhar et al. [21].

3.2 Temperature optimization

The deposition temperature of the ALD process is a critical parameter for successfully depositing the dielectric films with good electrical properties. In this work, the deposition temperature is restricted to below ∼120 °C because of the films application as gate dielectrics on topological insulators, which are thermally sensitive and degrade if heated to elevated temperatures for a prolonged time. As discussed in Sec. 3.1.3, there exists a temperature window in which the optimal growth occurs. However, for the precursors used in this study, it is expected to be observed at temperatures above our thermal restrictions [19].

The growth-per-cycle (GPC) was measured by ellipsometry for different temperatures between 60 °C and 120 °C at purge times of 60 s. This purge time is relatively long for a

standard ALD process and was chosen to remove all residual reactants after each process step. All depositions used 300 ALD cycles, resulting in film thicknesses between 17.5 nm and 35.4 nm. Excluding the initial two depositions, which demonstrate the highest and lowest growth rates, the range spans from 18.1 nm to 27.8 nm. This corresponds to a growth rate of (0.87 ± 0.10) Å per cycle which is considerably lower than observed by others in the same temperature range, where a GPC of ∼1.0 Å/cycle to ∼1.6 Å/cycle is measured [19, 21, 24–26]. As seen in Fig. 3.3 (left), no significant temperature dependence can be observed at 60 s purge time. Other studies, found a slightly decreasing GPC with increasing temperature in this temperature range [21, 27]. The deposition temperature is set to 80 °C for the subsequent depositions.

3.3 Precursor purge time optimization

The purge time between precursor pulses is a crucial parameter for achieving saturated growth at low temperatures [21]. Since the growth rate did not show significant changes with deposition temperature, the effect of different purge times was tested at 80 °C deposition temperature, with purge times from 30 s to 120 s. As seen in Fig. 3.3 (right), the growth rate exhibits a saturating behavior at purge times greater than ∼75 s. The saturated growth rate at 80 °C is (0.61 ± 0.10) Å/cycle. Shekhar et al. observed saturating behavior above 150 s purge times at 30 °C [21], while Kim et al. observed it above 50 s at the same temperature of 30 °C [27]. The saturated growth rates in those reports are 1.6 Å/cycle and 2.1 Å/cycle respectively. The difference in minimum purge times in different studies is predominantly linked to the specific reactor geometry and the purge gas flow rate. Therefore, the specific values can not be directly compared. Again, the GPC measured in our HfO_x depositions is considerably lower than in other studies.

Given that the dependence of GPC on purge time was much larger than that on deposition temperature, the purge time was selected as the variable for fabricating devices for electrical characterization. Additionally the temperature of 80 °C is the highest possible temperature where we are sure that it is not degrading the quantum anomalous Hall insulator during deposition.

In this chapter, the ALD deposition temperature was shown to have a negligible effect on

the growth rate, while a saturating behavior was observed with increasing purge times, leading to a saturated growth rate of $(0.61 \pm 0.10)\,\text{Å/cycle}$. After discussing the ALD process and its optimization, regarding the purge time and deposition temperature, the following chapter will address the electrical characterization of the grown films, where the relative permittivity ϵ_{r}, breakdown field E_{bd}, and the resistance R of the hafnium oxide films are determined.

4. Electrical Characterization of HfO_x films

Electrical characterization is a crucial step for assessing the quality of the HfO_x films deposited through ALD. To investigate the electrical properties of the deposited films, microelectronic devices are fabricated. Specifically, chips with capacitors of different sizes that utilize HfO_x as their dielectric material, are fabricated in a cleanroom.

The most important property is the relative permittivity (or dielectric constant) ϵ_r of the material, which is determined through capacitance measurements on the fabricated devices. The second property of interest is the breakdown electric field E_{bd}, which describes the maximum potential difference the film can withstand before becoming conductive and eventually being damaged. This is obtained by measuring the *IV curve* (current-voltage characteristic) of the device.

4.1 Device fabrication

The structures are fabricated in a cleanroom on $(7 \times 7)\,mm^2$ silicon substrates via multiple lift-off processes. The silicon substrates are cut from a 3-inch (100) silicon wafer.

The lift-off process is an additive method for creating patterns of a material on an underlying surface. It involves coating the substrate with a temporary layer, in this case, a photoresist, onto which the desired pattern is written by photolithography. In this work, a positive photoresist is used, which alters its composition in exposed areas, creating an inverse of the actual pattern. Afterwards, the photoresist is developed in a TMAH solution. This removes the parts previously exposed to UV light. A layer of material is then deposited over the entire surface, only coming into direct contact with the sample in the patterned area, where the photoresist has been removed. In the final step, the ac-

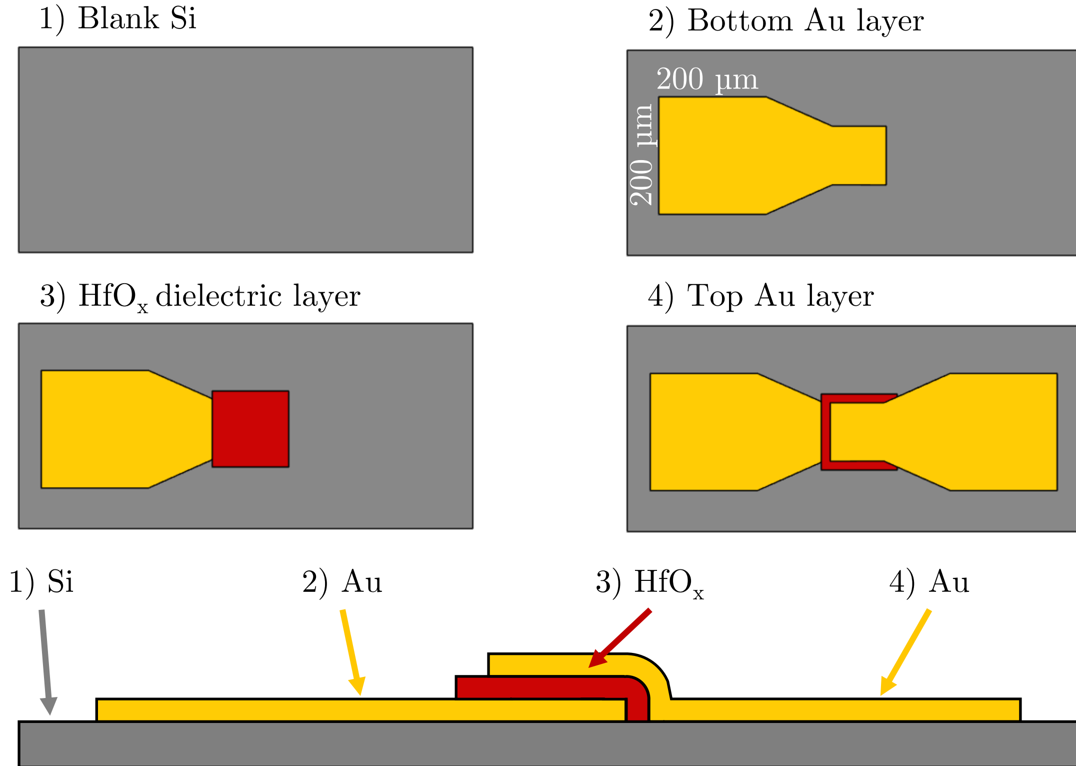


Fig. 4.1: 3D schematic diagram of the fabrication steps of the capacitors, layer thicknesses not to scale. 1) Blank silicon substrate, 2) bottom layer of (5 nm Pt/30 nm Au), 3) HfO_x dielectric layer, 4) top layer of (5 nm Pt/30 nm Au). The schematic on the bottom shows the stacking of the different layers.

tual lift-off step, the photoresist is dissolved in N-Methyl-2-pyrrolidone (NMP), a strong solvent. This lifts off the deposited layer in places where it does not directly touch the sample below, leaving behind the deposited film in the desired pattern.

The fabricated devices are composed of three layers, which are deposited subsequently and are patterned through the lift-off method. The top and bottom layers are made from 5 nm of platinum followed by 30 nm of gold. These layers serve as the capacitor plates and the ohmic contacts for probing and are deposited by sputtering. The intermediate layer is the dielectric hafnium oxide film, deposited by ALD, with thicknesses ranging from 20 nm to 30 nm. On each chip, twenty capacitors with areas ranging from $(10 \times 10)\,\mu m^2$ to $(200 \times 200)\,\mu m^2$ are fabricated.

The step-by-step fabrication process is described in Appendix B. The Layout used for the lithography was created with *KLayout* and is shown in Appendix B in Fig. B.1.

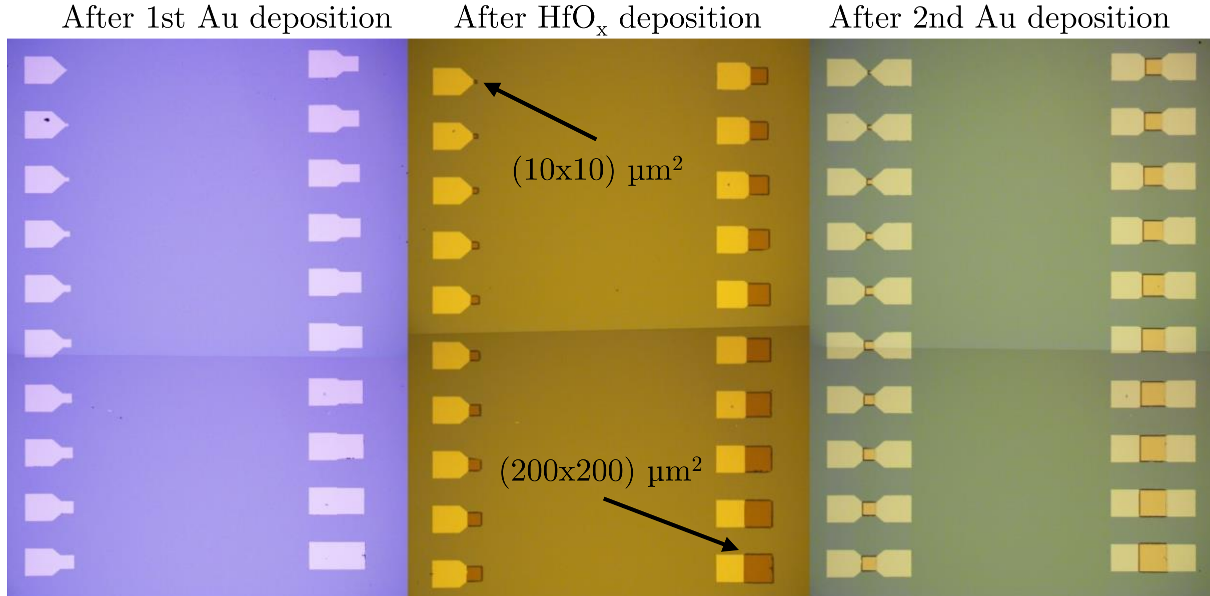


Fig. 4.2: **Microscope images of the capacitor chips after depositing:** (left) the bottom gold layer; (center) the HfO_x layer; (right) the top gold layer. The image on the right shows the finished device. Horizontal lines result from joining two images, and different colors are due to microscope settings.

With the exception of the HfO_x deposition, all process steps are conducted in a clean-room environment. Fig. 4.2 shows microscope images after depositing each of the three layers. Whenever a hafnium oxide layer is deposited for one of these chips, a clean and unpatterned silicon chip is placed inside the ALD reactor along with the actual device, such that the film thickness of exactly this deposition can be measured afterward. This ensures, that the data obtained through electrical characterization can be precisely converted from dimensionally dependent quantities to material-specific quantities.
Throughout the thesis, seven functioning capacitor chips were fabricated. Most of them only vary in their ALD deposition parameters. For control experiments (see Sec. 4.4), one device was fabricated with aluminum oxide Al_2O_3 as a dielectric layer, and another device was fabricated with ohmic contacts consisting of (40 nm Pt) instead of the (5 nm Pt/30 nm Au) combination used on all other chips. The devices fabricated are listed in Table 4.1. Film thicknesses are determined through ellipsometry for HfO_x dielectric. The Al_2O_3 dielectric was deposited in a different ALD reactor by my supervisor T. Röper and its thickness is only estimated and not measured.

Table 4.1: List of capacitor devices fabricated during the thesis

Name	C2	C3	C4	C5	C6	C7	C9
Dielectric material			HfO_x			Al_2O_3	HfO_x
Ohmic contacts			Pt+Au				Pt
ALD temperature [°C]			80			-	80
ALD purge times [s]	120	30	75	45	90	-	90
Dielectric film thickness [nm]	17.8	30.7	18.6	25.4	28.3	∼25	18.3

4.2 Probe stations and first assessment

Two probe stations are used during this work, one of them operating at room temperature and ambient pressure while the other one operates in a vacuum of less than 10^{-6} mbar at temperatures as low as 4 K. The two different probe stations are shown in Fig. 4.3. The room temperature probe station is an *MPI TS150* manual probe system by the *MPI Corporation*. The cryogenic probe station is a liquid helium flow cryostat by *Janis Research*, now part of *Lake Shore Cryotronics*. To rapidly assess whether the deposition and fabrication processes were successful and to easily spot non-functional, e.g. short-circuited, capacitors on the device, the probe station operating at room temperature and ambient pressure is used.

Short circuits in these capacitors are a result of defects in the hafnium oxide dielectric layer leading to direct contact between the top and bottom gold layers. These defects may be caused by contaminations or impurities introduced during fabrication, or an overly aggressive lift-off process that partially removed the HfO_x layer.

The probe station is connected to a *Keihtley 2450* sourcemeter in a simple two-point measurement setup, which is configured to source a voltage of 10 mV and measure the resulting output current with a limit of 100 nA, to avoid damaging the sample. After placing both tips of the probe station on the contact pads of a capacitor, the resulting current and voltage are read of the sourcemeter. This process is repeated for every capacitor on a chip. A capacitor is declared shorted only if no significant voltage (<1 mV)

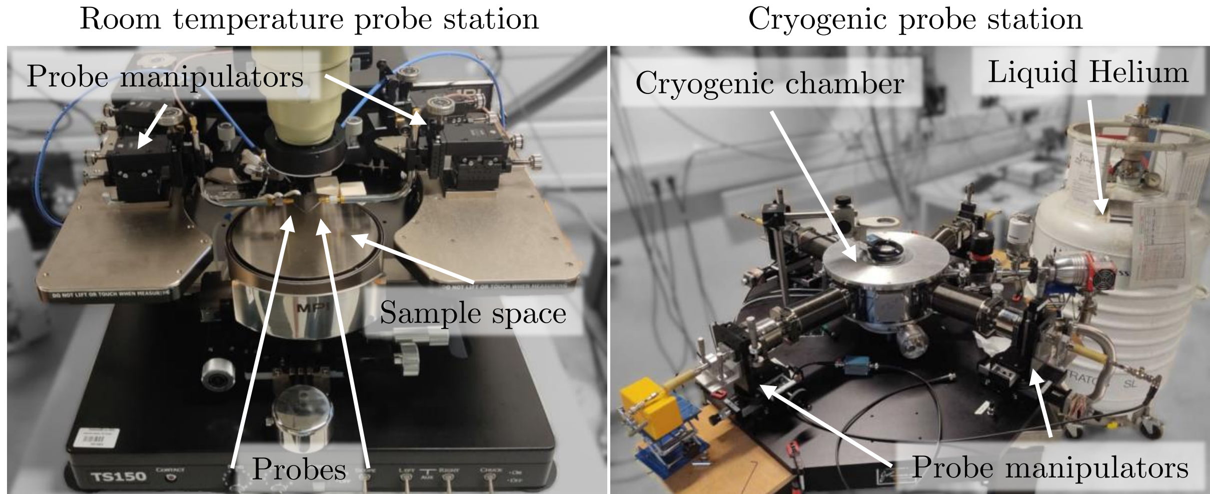


Fig. 4.3: (left) **Room temperature probe station:** The sample is placed on the circular table and contacted by two probes on the left and right, which can be precisely positioned using micrometer screws. (right) **Cryogenic probe station:** The sample is located within an inner chamber inside the visible metal chamber, isolated against heat transfer by a vacuum. The chamber is cooled by liquid helium from the white can on the right. The probes are manipulated and connected through the four ports and arms on each side of the chamber.

can be sustained at 100 nA of current, giving a minimum resistance of only 10 kΩ for a capacitor to be worth testing at low temperatures. This minimum acceptable resistance is chosen relatively low, as the hafnium oxide films demonstrate optimal insulating properties only at low temperatures. Additionally, the silicon substrate itself shows increased conductivity when exposed to visible light, as in the room temperature probe station, due to the photo effect.

4.3 Permittivity of HfO_x

4.3.1 Measurement setup and circuit model

To determine the relative permittivity ϵ_r of the hafnium oxide films deposited in this work, the capacitances of the devices are measured. This is done by applying an AC voltage U_{in} to a known resistor R_1 in series with the capacitors (modeled as a parallel

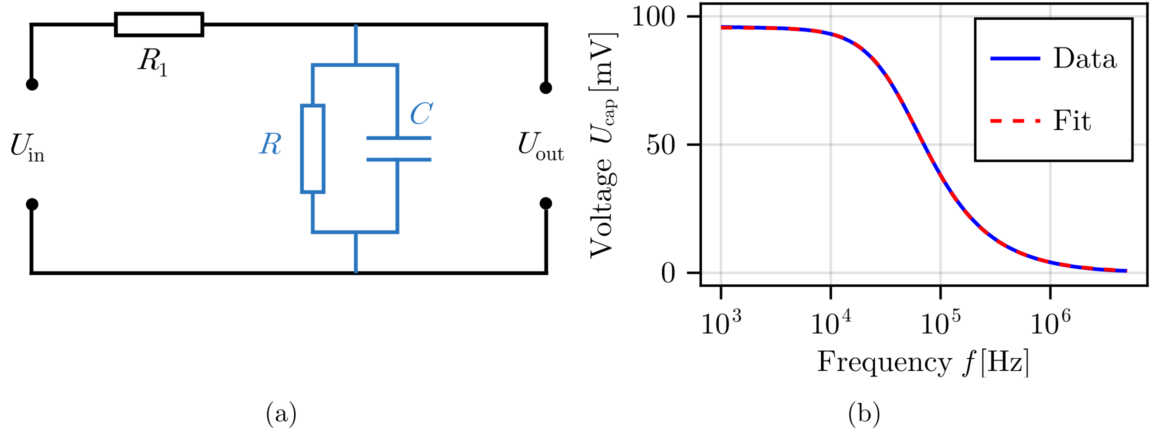


Fig. 4.4: (a) Schematic diagram of the circuit used to determine the capacitance of HfO_x films. The film is modeled as a capacitance C and a leak resistance R in parallel shown in blue. The resistor R_1 is known. The capacitance includes the capacitance of the HfO_x as well as the parallel line capacitance ($C = C_{HfO_x} + C_0$). (b) Absolute voltage across the capacitor as a function of input-voltage frequency at 100 mV amplitude. The data is fitted with a model representing the circuit in (a). The measurement is from capacitor 18 on chip C6 and was carried out at room temperature with $R_1 = 10\,\mathrm{k\Omega}$.

capacitance C and leak resistance R) and measuring the voltage drop U_{cap} across the capacitor while varying the input voltage frequency f. The resulting curve of U_{cap} as a function of frequency f, is fitted with a suitable model, revealing the capacitance C. Fig. 4.4 (a) shows the measurement setup as a schematic diagram. The blue part represents the hafnium oxide film, while R_1 represents the known resistor. Both voltage sourcing as well as voltage measurements are handled by a lock-in amplifier. The source voltage amplitude is set to 100 mV (rms), while the frequency range is 100 Hz to 1 MHz and 1 kHz to 5 MHz for a series resistance of 1 MΩ and 10 kΩ respectively.

The lock-in amplifier is a type of amplifier that detects phase-resolved signals of a known frequency from the measured input signal. This involves multiplying the signal by a pure signal of the desired frequency and integrating over time. By using a sufficiently long integration period, the process effectively filters out all other frequency components, isolating the frequency of interest. Thus, even in low signal-to-noise ratio environments, very small signals can be reliably detected [28]. The instrument used in this work is an

MFLI lock-in amplifier from *Zurich Instruments.*

When modeling the hafnium oxide film as a capacitance and a resistance in parallel, the relation between the voltage drop over the capacitor U_{cap} and the frequency of the input voltage f is described by Eq. 4.1.

$$U_{\mathrm{cap}}(f) = U_{\mathrm{in}} \frac{z_{\mathrm{cap}}}{Z} = \frac{U_{\mathrm{in}}}{\frac{R_1+R}{R} + i(2\pi f)CR} \tag{4.1}$$

The obtained lock-in data as well as the fit are shown for a representative capacitor in Fig. 4.4 (b). During this thesis, the absolute value of the measured voltage is fitted. The correspondence between the data and the fit is very good, validating the fit model used here. To verify the results, the complex phase calculated from the fit parameters is compared to the measured phase, showing close correspondence as well. These measurements are carried out at both room temperature and around 4 K. For measurements at low temperatures, where the hafnium oxide films exhibit high resistances, a series resistor of 1 MΩ is selected. For measurements at room temperature, a 10 kΩ resistor is used. At low temperatures, the leakage resistance of $\mathrm{HfO_x}$ is significantly larger than 10 kΩ, leading to almost no voltage drop across the series resistor, thereby making it difficult to accurately determine the resistance of the hafnium oxide. Room temperature measurements are performed on both probe stations to validate the data.

The results are capacitance and resistance values for capacitors of different capacitor areas. Since the measured capacitances are composed of the line capacitance and the actual film capacitance, the resulting values are plotted against the respective capacitor area leading to data of the form $C(A)$. Since the line capacitance is constant, this data can be fitted with a linear function representing

$$C(A) = C_0 + \frac{\epsilon_0 \epsilon_{\mathrm{r}}}{d} \cdot A \tag{4.2}$$

where C_0 is the line capacitance, d is the film thickness, ϵ_0 the vacuum permittivity and ϵ_{r} the relative permittivity of the $\mathrm{HfO_x}$ film. Through this process, the relative permittivity of each device can be obtained. To further validate these results, for each device, the same measurement technique was applied to a measurement of just the silicon substrate, where the tips of the probe station were placed on the contact pads of two adjacent capacitors, thus measuring only the line capacitance and silicon substrate capacitance. These were

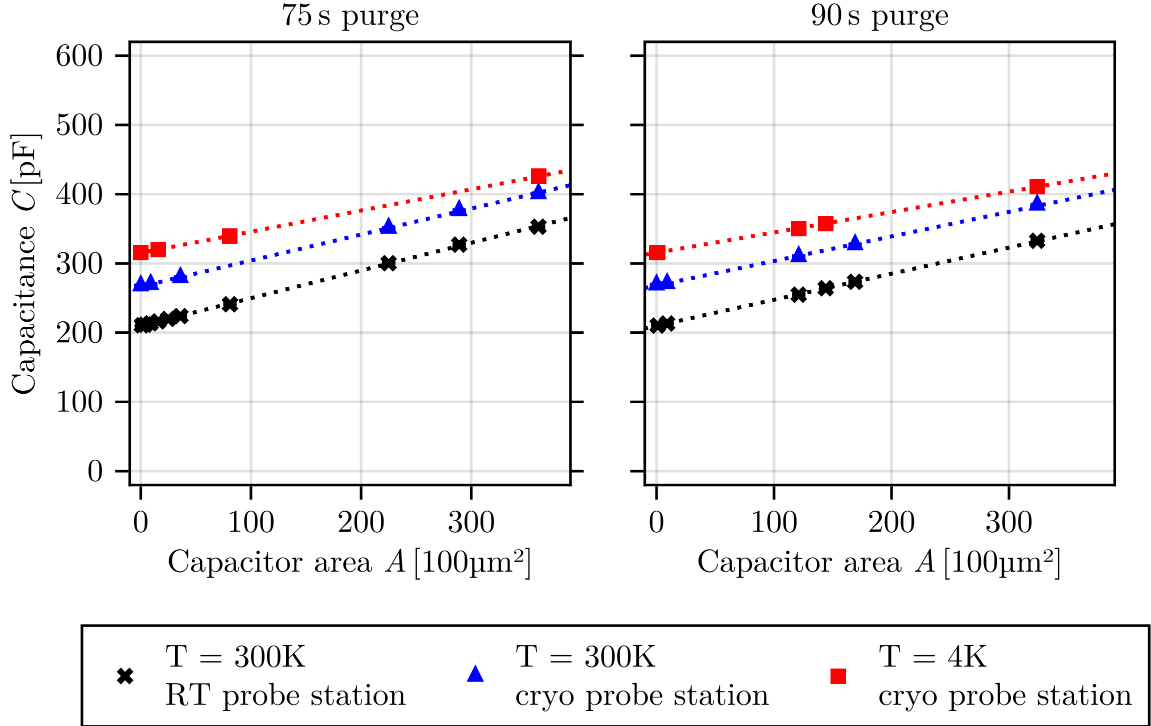


Fig. 4.5: Capacitances as a function of capacitor area for two different devices C4 and C6. Dotted lines represent linear fits, whose slope is proportional to ϵ_r. The different colors correspond to different measurement environments.

included in the linear fit as capacitors with $A = 0$ and therefore only representing the y-axis intercept C_0.

The resistance values for each capacitor on a device should follow the form

$$R(A) = \frac{1}{\frac{1}{R_{\mathrm{HfO_x}}(A)} + \frac{1}{R_{\mathrm{Si}}}} = \frac{1}{\frac{A}{\rho d} + \frac{1}{R_{\mathrm{Si}}}} \tag{4.3}$$

with R_{Si} the silicon substrates resistance, parallel to $R_{\mathrm{HfO_x}}$, ρ the specific resistivity of the dielectric layer, d the layer thickness and A the capacitors area. The measurements of the bare silicon substrate were included in the fit as capacitors with area $A = 0$, therefore only representing R_{Si}.

4.3.2 Experimental results

The capacitance is measured for a representative sample of capacitors on each device. The primary measurement environment is at low temperatures in a vacuum, but to validate

the data, measurements are carried out in three different environments:

1. At room temperature and ambient pressure in the room temperature probe station
2. At room temperature and in vacuum in the cryogenic probe station
3. At 4 K and in vacuum in the cryogenic probe station.

All measurements are conducted in the dark to prevent conduction through the silicon substrate via photoconduction. The capacitances C as a function of capacitor area A are shown for chips C4 and C6 in Fig. 4.5. The relative permittivity ϵ_r can be extracted from the slopes of the linear fits, using Eq. 4.2. The capacitances on all devices align closely with a linear fit, supporting the validity of the measurements, although the slopes differ between the measurement environments. The relative permittivity values for each device and measurement setup are shown in Fig. 4.6 (a). At 4 K the relative permittivities of all devices are between 6 and 10. The largest relative permittivity is found at 90 s purge time, with $\epsilon_r \sim 9.4$, while the lowest value is found at 75 s purge time with $\epsilon_r \sim 6.4$. Although the different setups closely agree with each other, validating the accuracy of ϵ_r for a single device, no clear dependence of relative permittivity on the ALD purge time could be found. An additional device with an Al_2O_3 dielectric layer was measured as well, showing a permittivity of ~ 7. On all devices, ϵ_r increased by about ~25 % for measurements at room temperature. This increase in relative permittivity at increasing temperatures was observed by others as well [29]. In comparison with HfO_x layers deposited in other studies, the dielectric constant of our films is considerably lower. Shekhar et al. found a relative permittivity of ~ 15 in their layers deposited at 30 °C [21], Kim et al. observed a value of ~ 16 for layers grown at 100 °C [27], while Gieraltowska et al. measured their films to have a relative permittivity of ~ 17 at 85 °C [25]. Additionally Gieraltowska et al. found a strong decrease of the dielectric constant with respect to film thickness, from ~ 22 at 200 nm thickness to ~ 14 at 20 nm [25]. All of those layers were deposited at the same 85 °C. Gieraltowska et al. link this dependence to an increase in crystallinity, grain size, and density of those films with increasing film thickness [25]. This fits our data, as our films had thicknesses of only 17 nm to 30 nm and also show a slight decrease of ϵ_r with decreasing film thickness. It should be noted, that the data shown in Fig. 4.6 (b) may

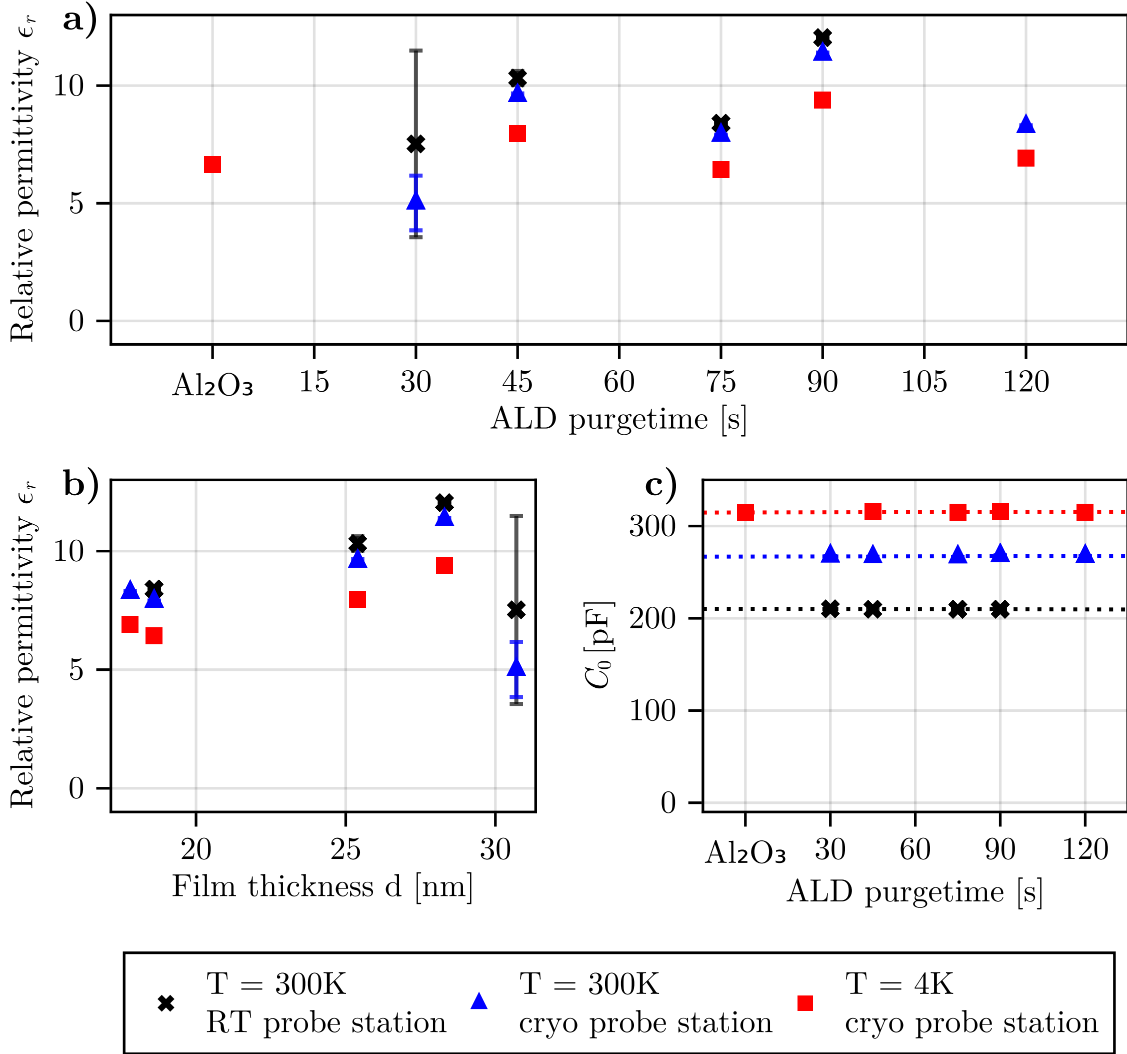


Fig. 4.6: (a) Relative permittivity ϵ_r as a function of ALD purge time. Different colors represent different measurement setups, with red squares indicating the central low-temperature measurement. Permittivities were calculated from the slopes of the fits of capacitance-vs-area data. (b) Data from (a) is presented as a function of film thickness. (c) y-axis intercept of the linear fits on different devices, representing the line capacitance C_0.

not be accurate, as the film thickness was altered through the use of different purge times and not a different number of ALD cycles. Since the structural properties of the HfO_x films were not measured in our work, the reason behind this decrease can not be confirmed. Fig. 4.6 (c) show the y-axis intercept of the linear fits, representing the line capacitance

C_0 as a function of ALD purge time. As expected, the data is constant between different devices with different HfO_x layers, supporting the accuracy of permittivity values. Lastly, the resistances obtained through fitting Eq. 4.1 to the lock-in measurements do not align with Eq. 4.3. For low-temperature measurements, all resistances (even from the bare silicon measurements) are just below $10\,\mathrm{M\Omega}$, while for room-temperature measurements, they are between $0.1\,\mathrm{M\Omega}$ and $1\,\mathrm{M\Omega}$. At $T = 4\,\mathrm{K}$, the actual resistances of the devices, determined through IV measurements, are about three orders of magnitude larger than measured here (see Sec. 4.4.2). As a result, the resistivity and substrate resistance values calculated by fitting the data are considered unreliable and will not be discussed in further detail.

4.4 Electric-field breakdown of HfO_x

4.4.1 Measurement setup

IV measurements were carried out, to investigate the breakdown electric field strength of the hafnium oxide thin films. The resulting IV curves refer to the relation between an applied voltage (V) and the resulting current (I) through the thin film. The voltages are cyclically ramped from 0 V to 25 V to −25 V and back to 0 V, while the current is limited to 10 nA to protect the devices. The breakdown voltage is determined as the voltage at which the current exceeds 1 nA. This voltage is then converted to a breakdown electric field E_{bd}, by dividing it by the film thickness. The breakdown is not determined by surpassing a threshold in *current density*, as the electrical breakdown is a localized effect that is not directly related to the capacitor area. Furthermore, the linear increase around 0 V is fitted to estimate the film resistance in that voltage range. The IV curves with marked breakdown voltages of a sample of devices are shown in Fig. 4.7. The measurement was performed with the *Keithley 2450* sourcemeter, connected to the capacitor via the probe station in a two-point measurement setup. Since these films are intended to be used as gate dielectrics in topological insulator devices, which will be tested and analyzed at temperatures near absolute zero, the IV measurements were conducted in the cryogenic probe station in a high vacuum environment at temperatures between 4 K and 10 K.

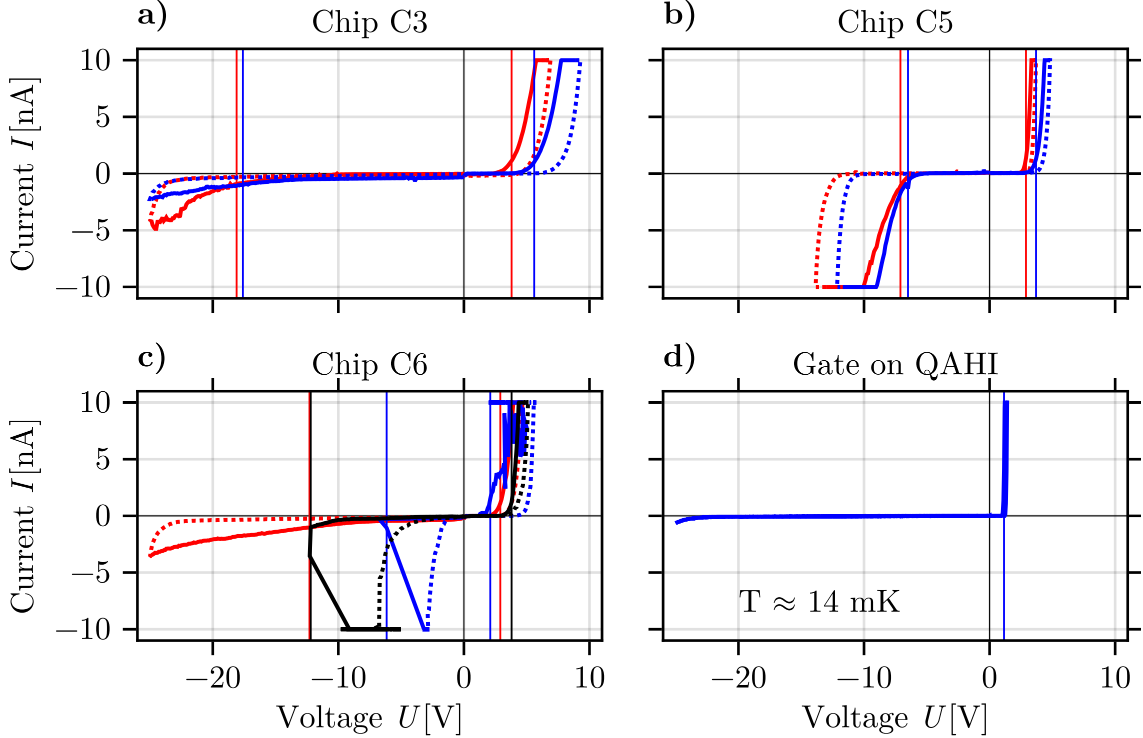


Fig. 4.7: a-c) Example IV curves for capacitors on chips C3, C5, and C6, taken at $T \approx 4\,\mathrm{K}$. Solid lines indicate increasing voltage magnitude, while dotted lines denote decreasing voltage magnitude. Breakdown voltages are marked by vertical lines. d) IV curve of HfO_x as a gate dielectric on a QAH insulator, taken at $T \approx 14\,\mathrm{mK}$. The gate oxide was deposited at 80 °C and 90 s purges, the same conditions as chip C2. This measurement is discussed in more detail in Chapter 5

4.4.2 Experimental results

All IV curves obtained exhibit pronounced hysteresis and asymmetry. The asymmetry is characterized by an IV curve that, on one side, abruptly and rapidly reaches the current limit, similar to the behavior of a diode. The breakdown voltages differ significantly between the positive and negative sides, with the breakdown occurring much earlier on one side. The terms *positive* and *negative* are relative here, as they depend on which side of the capacitor is connected to the negative terminal of the sourcemeter, which was not the same for all measurements. Surprisingly, the breakdown always appears at lower voltages, if the higher potential is at the top electrode of the capacitor devices. Consequently, all

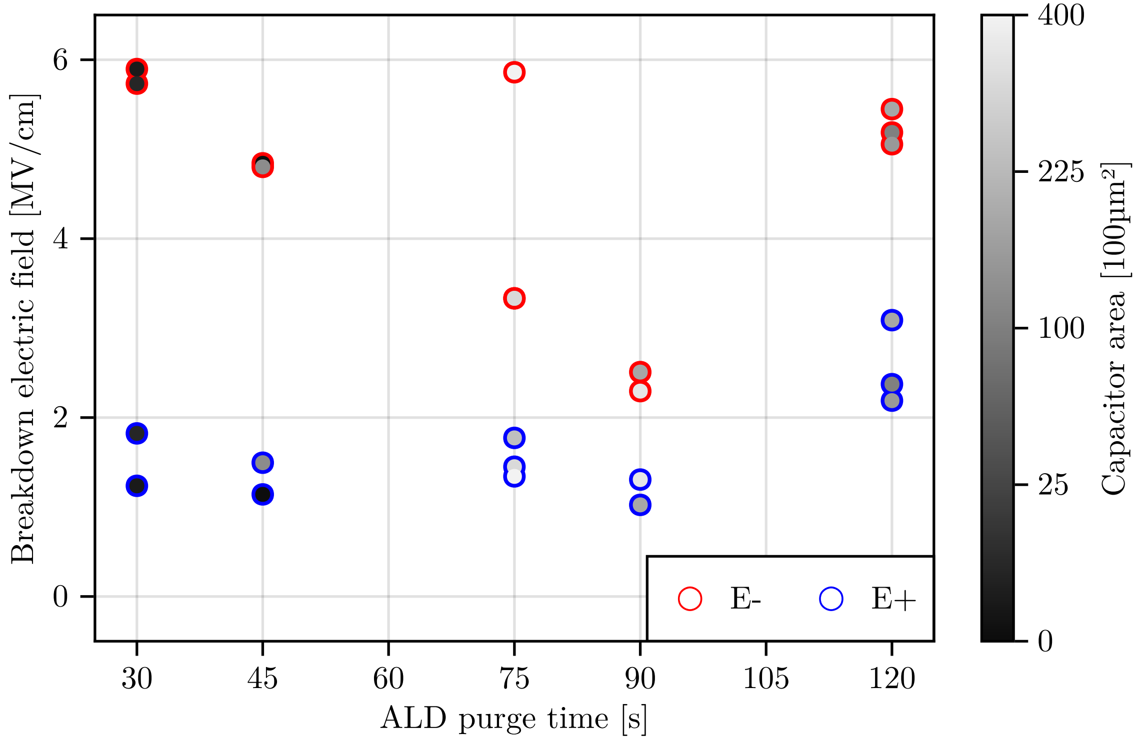


Fig. 4.8: Breakdown electric fields E_{bd} of all devices with HfO_x dielectric. Each pair of red and blue circles represents an IV measurement on one capacitor. The circle's border distinguishes between positive (blue) and negative (red) electric breakdown fields, while its interior color approximates the dielectric area of the capacitor. Measurements were taken between 4 K and 10 K.

IV data is adjusted such that the earlier breakdown appears at positive voltages for comparability. Interestingly, the asymmetry increased drastically at even lower temperatures, as seen in Fig. 4.7 (d). The measurement was taken on a QAH insulator (see sample of Chapter 5) at $T \approx 14\,\text{mK}$ and shows no breakdown until $-25\,\text{V}$ on the negative side, while breaking down at $\sim 1\,\text{V}$ for positive voltages.
To compare the breakdown between different devices, the breakdown voltage is converted into a breakdown electric field strength. The breakdown electric field for the diodic side (blue circles in Fig. 4.8) is near constant at $E_{bd} \sim 1.5\,\text{MV}\,\text{cm}^{-1}$, except for the device with 120 s of ALD purge time. The breakdown electric field for negative voltages is considerably higher at $2\,\text{MV}\,\text{cm}^{-1}$ to $6\,\text{MV}\,\text{cm}^{-1}$. No clear dependence on ALD purge time can be seen in the obtained data. The range of approx. $1 - 6\,\text{MV}\,\text{cm}^{-1}$ is coherent with other

studies [25, 30]. Gieraltowska et al. found a breakdown field of ~1 $\mathrm{MV\,cm^{-1}}$ for the same layer thickness and deposition temperature as in our work [25].
The second surprising discovery was the hysteresis, which appeared on both sides of the IV curves, although it was much more pronounced at negative voltages. For positive voltages, where diodic behavior occurs, the hysteresis manifests as a shift of the curve of ~1.5 V to higher voltages on the return path. When sweeping from 0 V to −25 V, the current increases gradually until it reaches the current limit, while on the sweep back to 0 V, it falls much steeper, forming a hysteresis loop. On two IV curves on Chip C5, shown in Fig. 4.7, the current starts to rise gradually, but suddenly jumps to the current limit.
To further investigate the asymmetric and hysteretic behavior and its origins, additional devices were fabricated. The fact that the breakdown always occurred earlier, when the higher potential is at the top electrode suggests that the asymmetry (at least partially) stems from asymmetric device geometry and the different interfaces of Au-HfO_x and HfO_x-Pt at the bottom and top electrode respectively. Owing to the different work functions of Au and Pt, this might lead to an asymmetric barrier. To verify this, a symmetric capacitor (Pt-HfO_x-Pt) was fabricated. Furthermore, a conventional capacitor device was fabricated, using Al_2O_3 instead of HfO_x dielectric. Additionally, IV curves on a conventional HfO_x device were measured at different voltage ramp rates ranging from 0.01 $\mathrm{V\,s^{-1}}$ to 1 $\mathrm{V\,s^{-1}}$ to investigate the hysteretic behavior. All measurements carried out to study the asymmetry and hysteresis are shown in Fig. 4.9. When comparing the different ohmic contacts, Fig. 4.9 (left), both positive and negative breakdown voltages are significantly larger, but the asymmetry does not change, with the breakdown still occurring much earlier at positive voltages. A possible explanation for this asymmetry is the formation of an interface layer during the first few ALD cycles, which could have a different work function than the HfO_x deposited in the last few cycles. A different interface at the top and bottom electrode of a Pt-HfO_2-Pt capacitor was also found by Kang and Park, who observed asymmetric current-voltage relations as well [31].
Regarding the hysteresis, the IV curves taken with varying voltage ramp rates show a slight shift of the breakdown to higher voltages, if the ramp rate is increased. The IV curves of a capacitor with Al_2O_3 dielectric look much less asymmetric, although the

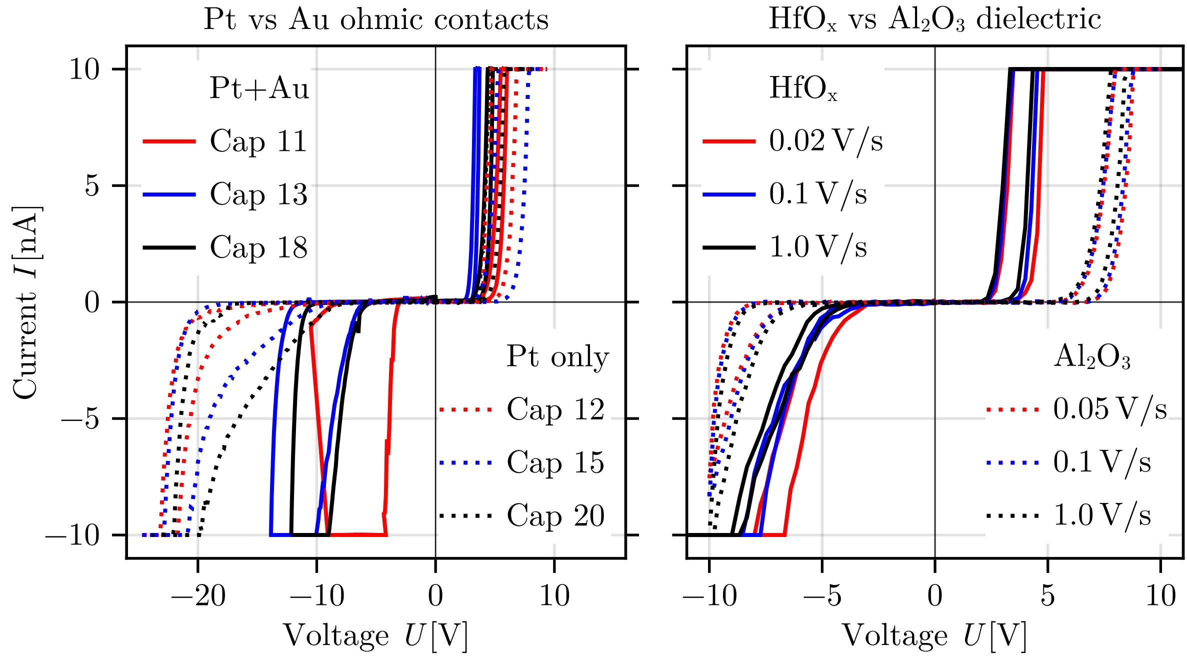


Fig. 4.9: (left) Comparison of IV curves of two devices with different ohmic contacts (40 nm Pt vs 5 nm Pt + 30 nm Au) but with the same HfO_x layer deposited at 80 °C with 60 s purge times. (right) Comparison of IV curves between capacitor 19 on device C4 with an HfO_x dielectric layer and capacitor 11 on device C7 with an Al_2O_3 dielectric layer. The IV curves are taken at different ramp rates to investigate the influence of the sweeping speed.

breakdown still occurs $1 - 2$ V earlier on the positive side.

In summary, both asymmetry and hysteresis can not be fully explained with the data measured. The asymmetry may be caused by an interface layer, which could be further investigated by fabricating devices with different dielectric thicknesses. In general, thicker dielectric layers could facilitate the study of electric field breakdown, as the dielectrics are less likely to suddenly break down through point defects as seen in Fig. 4.7 on Chip C6. Finally, the resistances derived from fitting the linear region around 0 V are discussed. Linear regions for positive and negative voltages are fitted separately and averaged afterward, as the IV curves often showed a slight vertical step at 0 V. All devices exhibit resistances between 40 GΩ to 250 GΩ, with no observable dependence on purge time. The resistances are larger than the sense input impedance of the sourcemeter, which is specified to be above 10 GΩ. While this compromises the precision of the exact

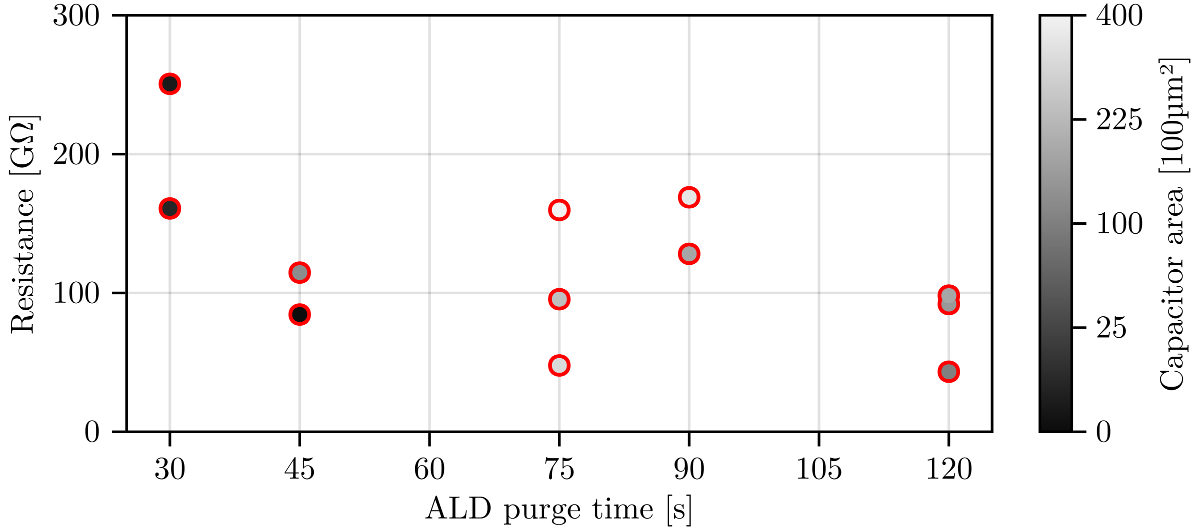


Fig. 4.10: Comparison of the resistances of different capacitors as a function of ALD purge time. The resistances are obtained by fitting the linear regimes of the IV curves.

resistance values, it confirms that the measurements are within the gigaohm range. For gate dielectrics, a leak resistance in the gigaohm range is sufficiently large to avoid issues with leakage current.

In conclusion, the hafnium oxide grown in this thesis is shown to have a relative permittivity ϵ_{r} of 6 to 9 at $T \approx 4\,\mathrm{K}$, with no observable dependence on purge time. At room temperature, the values increase by about ∼25 %. The electric-field breakdown is asymmetric with breakdown fields of $E_{\mathrm{bd}} \sim 1.5\,\mathrm{MV\,cm^{-1}}$ if the higher potential is at the top electrode and $E_{\mathrm{bd}} \sim 2 - 6\,\mathrm{MV\,cm^{-1}}$ in the opposite case. Again, no dependence on purge time is observed. The resistances were determined through two different methods, both at temperatures of $T \approx 4\,\mathrm{K}$. Resistances obtained by I-V measurements are between 40 GΩ and 250 GΩ. The second method calculated the resistances by fitting the lock-in data obtained in the permittivity measurements. For all devices and capacitors, those values were just below 10 MΩ, indicating that the measurement process is not suitable for resistances in the gigaohm range. In the following chapter, the application of the $\mathrm{HfO_x}$ films for gating purposes on a quantum anomalous Hall insulator is demonstrated, including the fabrication of QAH samples, the measurement setup, and experimental results.

5. Application as a gate dielectric on QAHIs

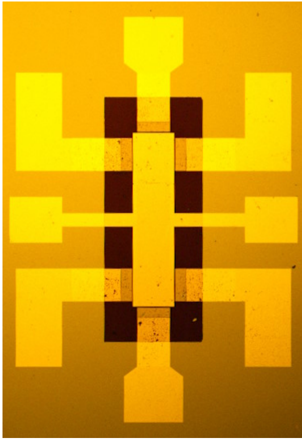


Fig. 5.1: Microscope image of the finished QAH device. The dark rectangle shows the dielectric.

The HfO_x film deposited at 80 °C and with purge times of 90 s is applied as a gate dielectric on a quantum anomalous Hall sample. The QAH insulator used to confirm and investigate the gate effect is vanadium doped $(Bi_xSe_{1-x})_2Te_3$ (V-BST). V-BST is grown by molecular beam epitaxy (MBE) on an Indium Phosphide (InP) substrate in the research group of Prof. Yoichi Ando (II. Institute of Physics, University of Cologne). Since the V-BST degrades if exposed to ambient air for prolonged times, the V-BST layer is capped with a layer of Al_2O_3 after deposition. The QAH measurement sample uses the Hall bar geometry shown in Fig. 5.1 and with more detail in Fig. 5.2, and is fabricated through multiple etching, lithography, and deposition steps. The gold gate electrode and ohmic contacts as well as the HfO_x dielectric layer were fabricated with the same processes and parameters explained in Sec. 4.1 and Appendix B. All other fabrication steps, such as etching the Hall bar geometry into the V-BST, were conducted by my supervisor T.Röper and are not discussed in this work. The ALD deposition consisted of 300 cycles, resulting in a film thickness of $\sim$ 19 nm. Six Hall bar structures were fabricated on a device, each of which was probed at room temperature, to assess its quality. After fabrication, the device is mounted to a *QDevil Q102* daughter board, a standardized sample holder. The most promising Hall bar's contact pads are connected to the sample holder by thin metal wires attached by wire bonding.

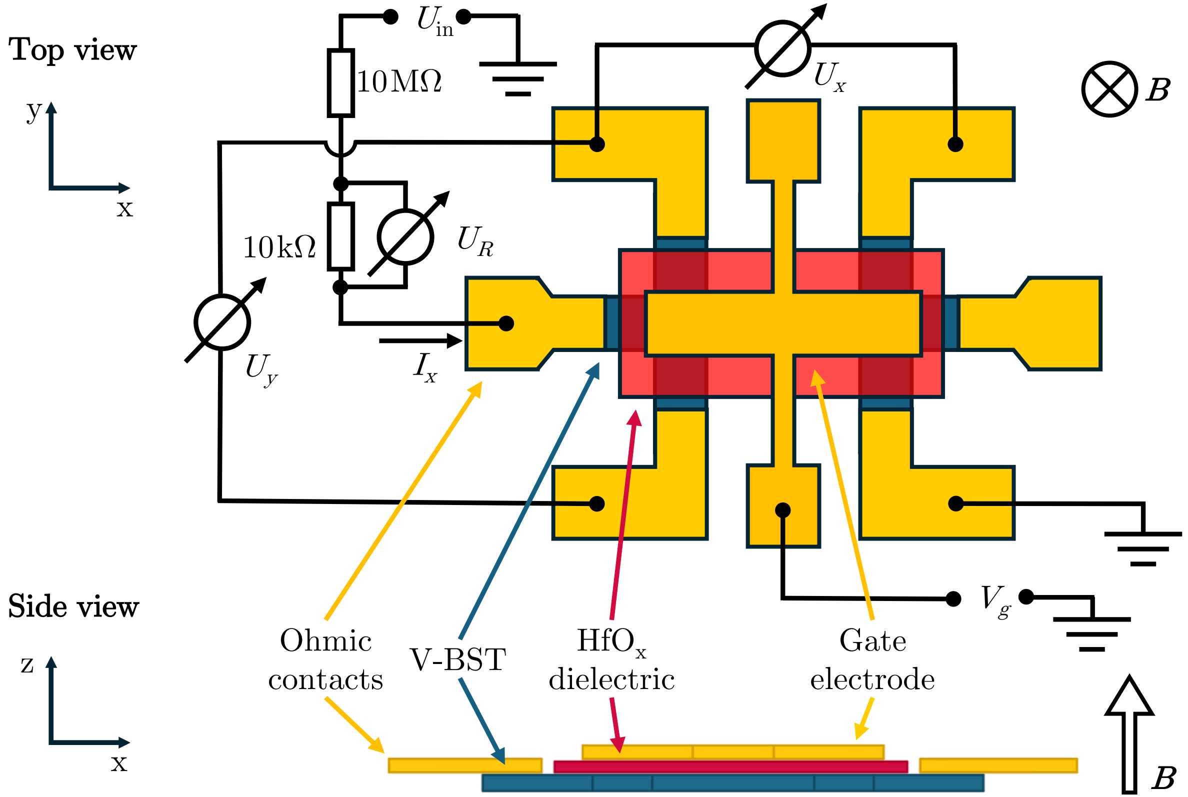


Fig. 5.2: Schematic diagram of the quantum anomalous Hall (QAH) measurement setup. The top view illustrates the V-BST Hall bar (blue), with gold components (yellow) representing the gate electrode and ohmic contacts for probing. The HfO_x gate dielectric (red) is made partially transparent for better visibility. The side view displays the device's layer stacking. During measurements, a constant current $I_x \approx 1\,\text{nA}$ is applied along the x direction by supplying a voltage $U_{\text{in}} = 10\,\text{mV}$ to the $10\,\text{M}\Omega$ resistor, which is much larger than the other resistances in series. The actual current is determined from the voltage drop U_R over the $10\,\text{k}\Omega$ resistor in series with the Hall bar. The Hall resistance $R_{xy} = U_y/I_x$ is calculated using the Hall voltage U_y, while the longitudinal resistance $R_{xx} = U_x/I_x$ is obtained from the longitudinal voltage U_x. An out-of-plane magnetic field B can be applied along the z-axis to control the sample's magnetization. The gate voltage V_g can be applied to either of the gate electrode's ohmic contacts. The setup shown here is not ideal, as the right-most contact should be grounded instead of the bottom-right to have a fully symmetric setup. This was not possible due to a faulty bonding wire which made the contact unaccessible.

The measurement is conducted in an ultra-low temperature dilution refrigerator by *Bluefors* because the V-BST used in this work exhibits the QAH at temperatures of $T \lesssim 200\,\mathrm{mK}$ [14]. The sample holder is mounted and connected to the refrigerator such that it is oriented perpendicular to the magnetic field of an electromagnet inside the cooling system.
The measurement instruments used are three lock-in amplifiers, a Keithley sourcemeter, and the electromagnet. The magnet is used to apply an out-of-plane magnetic field B_z between $-2\,\mathrm{T}$ and $2\,\mathrm{T}$ to control the sample's magnetization. Gate voltage V_g and gate leakage current are sourced and measured by the sourcemeter. The three lock-in amplifiers are synchronized. One of them supplies an input signal U_{in} to the device and the others are used for detection only. Each lock-in amplifier measures one of the voltages U_R, U_x and U_y shown in Fig. 5.2. By choosing an input voltage frequency $f = 7\,\mathrm{Hz}$, the setup approximates a DC measurement, while still benefiting from the higher accuracy compared to a DC measurement. The current I_x and the transverse R_{xy} and longitudinal R_{xx} resistances can be calculated from the measured voltages U_R, U_x, and U_y. Before measuring the quantum anomalous Hall effect, positive and negative breakdown voltages of the $\mathrm{HfO_x}$ dielectric are measured by cyclically ramping the gate voltage to identify a usable gate voltage range. In the positive voltage regime, the breakdown occurred at $\sim$1.5 V. For negative voltages, the leakage current did not reach 1 nA at the maximum voltage of $-25\,\mathrm{V}$, although a steeper increase in leakage current occurred between $-20\,\mathrm{V}$ and $-25\,\mathrm{V}$. This sets a usable gate voltage range $-25\,\mathrm{V} \leq V_g \leq 1\,\mathrm{V}$. The leakage current I_g as a function of gate voltage V_g is shown in Sec. 4.4 Fig. 4.7 (d). Between $-20\,\mathrm{V}$ and 1 V the gate showed a resistance of $(265 \pm 7)\,\mathrm{G\Omega}$.
During the first measurement, the transverse and longitudinal resistance R_{xy} and R_{xx} are recorded as a function of gate voltage, at magnetic field strengths of $-2\,\mathrm{T}$, $0\,\mathrm{T}$ and $2\,\mathrm{T}$. The objective is to identify the gate voltage range in which the sample's Fermi level resides within the energy gap. This voltage range in which the QAH can be observed is referred to as the *quantized regime*, where R_{xy} is quantized. In the second experiment, the gate voltage is set to a value within the quantized regime. R_{xy} and R_{xx} are recorded as a function of the magnetic field B, which is swept from $-2\,\mathrm{T}$ to $2\,\mathrm{T}$ and back to $-2\,\mathrm{T}$. The data obtained through both measurements is shown in Fig. 5.3. Both measurements

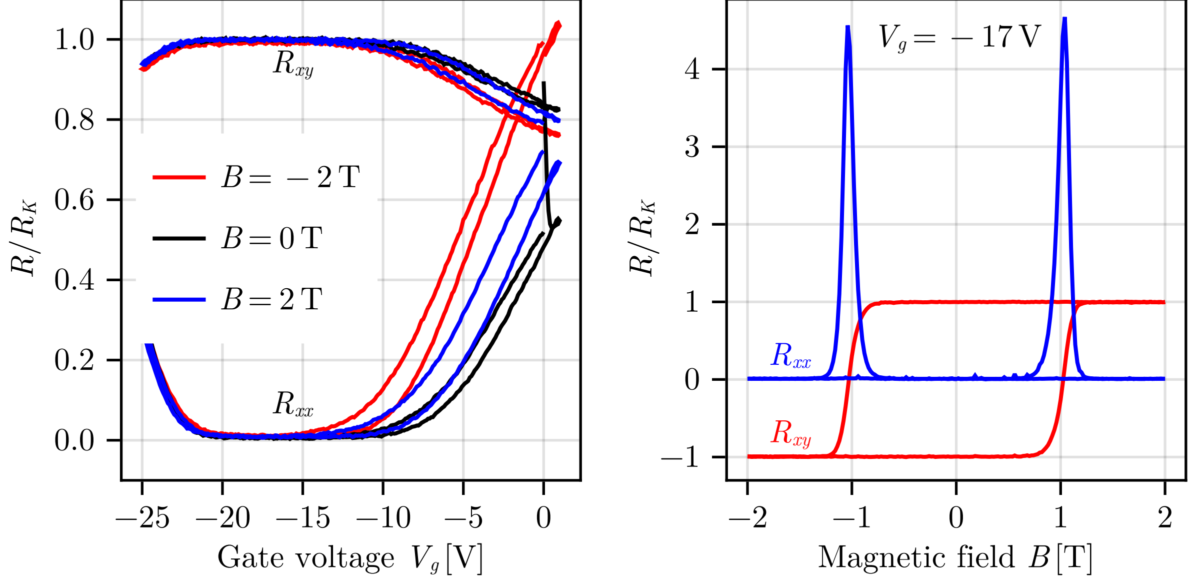


Fig. 5.3: QAH measurements at $T \approx 14\,\mathrm{mK}$ on a V-BST magnetic topological insulator using a gold gate and HfO_x gate dielectric. (left) Transverse R_{xy} and longitudinal R_{xx} resistance as a function of gate voltage at different magnetic field strengths, showing a quantized regime between $-20\,\mathrm{V}$ and $-15\,\mathrm{V}$. (right) Magnetic field sweep between $-2\,\mathrm{T}$ and $2\,\mathrm{T}$ while measuring R_{xy} and R_{xx} at $V_g = -17\,\mathrm{V}$. The sample exhibits the quantum anomalous Hall effect as described in Sec. 2.3. R_{xy} is quantized to $\pm R_K = \pm h/e^2$ and changes sign at the coercive fields. R_{xx} vanishes everywhere except for the coercive fields, at which it shows a pronounced peak.

show the expected results and confirm the gate effect on the sample. The gate voltage sweep shows a clearly defined quantized regime, in which the transverse and longitudinal resistance are fixed at R_K and zero respectively. The start and end points of this voltage range slightly depend on the magnetic field B, which is shown in more detail in Fig. 5.4. This is likely caused by the asymmetric current-sourcing shown in Fig. 5.2.

The gate sweep at zero magnetic field exhibits the most precise quantization of R_{xy} to $R_K = h/e^2$, with a deviation of only 0.029 %. The highest deviation in gate sweep measurements is recorded at $-2\,\mathrm{T}$ with 0.8 %. The field sweep showed a deviation of 0.4 %. Notably, all measurements of R_{xy} are below the value of R_K.

The longitudinal resistance R_{xx} was found to be between $150\,\Omega$ and $300\,\Omega$ for all measurements. Again, the gate sweep at $B = 0\,\mathrm{T}$ yielded the most accurate data, with

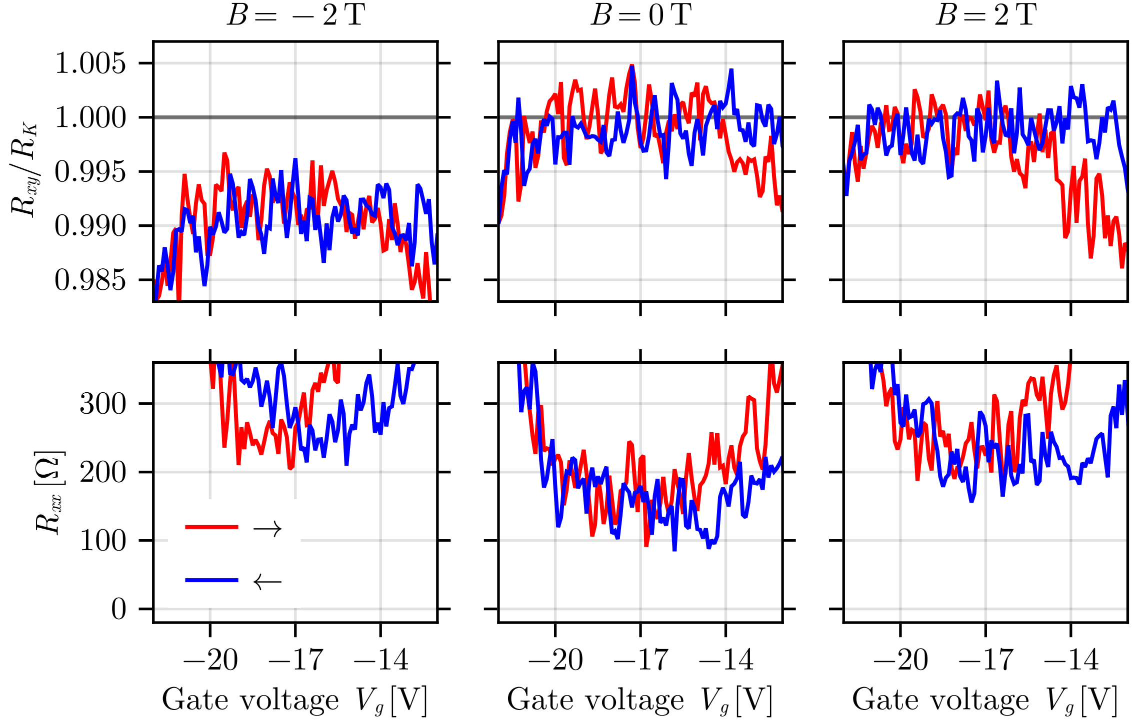


Fig. 5.4: Detailed view of the quantized regimes of the gate voltage sweep in Fig. 5.3. The top row shows R_{xy} in units of h/e^2 while the bottom row shows R_{xx}. Different columns correspond to different magnetic fields. Red curves indicate an increasing gate voltage while blue curves indicate a decrease. Asymmetry between $B = \pm 2$ T is most likely caused by the asymmetric current sourcing.

$R_{xx} = (158 \pm 25)\,\Omega$, while the measurement at $B = -2$ T resulted in the highest value, $R_{xx} = (277 \pm 28)\,\Omega$. All values of R_{xy} and R_{xx} along with details about how they were calculated are shown in Table C.1. Fig. 5.4 and Fig. 5.3 (a) show a slightly hysteretic behavior in R_{xy} and R_{xx} when comparing the measurements with increasing and decreasing gate voltage. The curves with increasing voltage exhibit a narrower quantized regime.

In this chapter, we successfully achieved the main goal of the thesis: Demonstrating the gate effect on thermally sensitive QAHIs with HfO_x deposited at low-temperature. Clear quantization of R_{xy} was observed while sweeping the gate voltage V_g, with a quantized regime between -14 V and -20 V for all measurements. In the same voltage range, the longitudinal resistance dropped to approximately 200 Ω. Additionally, a hysteresis curve describing R_{xy} during a magnetic field sweep was observed at $V_g = -17$ V.

6. Summary and Outlook

In this work, we optimized the low-temperature deposition of hafnium oxide, by varying crucial process parameters such as the deposition temperature and the precursor purge times. The process showed no significant temperature dependence between 60 °C and 120 °C. Therefore, and to avoid sample degradation, the deposition temperature was kept at 80 °C in the following depositions. Subsequently, the influence of purge time was investigated, showing a saturating behavior for purge times $\gtrsim 75\,\mathrm{s}$. The saturated growth rate per cycle (GPC) is measured at $(0.61 \pm 0.10)\,\text{Å}/\text{cycle}$, which is considerably lower than in other studies [19, 21, 24–26].

Relative permittivity ϵ_r and breakdown field strength E_bd were determined by applying the hafnium oxide grown at 80 °C as a dielectric in capacitors of different areas. By measuring the capacitances, the permittivity is shown to be between 6 and 10 at $T \approx 4\,\mathrm{K}$, with no clear dependence on the purge time. The electrical breakdown is strongly asymmetric with breakdown fields of $E_\mathrm{bd} \sim 1.5\,\mathrm{MV\,cm^{-1}}$ when the high potential is at the top electrode and $E_\mathrm{bd} \sim 2 - 6\,\mathrm{MV\,cm^{-1}}$ in the opposite case. The resistances of all measured capacitors are between $40\,\mathrm{G\Omega}$ and $250\,\mathrm{G\Omega}$, but do not show the anticipated dependence on the capacitor area. This is presumably due to the conduction occurring at low-resistance defects and not uniformly across the entire area. These results indicate a well-functioning dielectric, showing a comparatively high breakdown field strength and low leakage current as shown by the high resistances. The relative permittivity is lower than expected. However, it is still sufficiently high to achieve a significant gate effect as shown in Chapter 5.

Lastly the final goal of the thesis, namely gating a thermally sensitive QAH sample with hafnium oxide, was achieved (see Chapter 5 for more detail). We are able to tune the

QAH sample into its quantized regime by applying a gate voltage $V_g = -17\,\mathrm{V}$. At this gate voltage, the expected behavior of R_{xx} and R_{xy} can be demonstrated, verifying the gate effect.

In this thesis, we successfully deposited hafnium oxide at temperatures below 100 °C, showing a significant gating effect on a quantum anomalous Hall insulator, opening up the potential for further gating applications on temperature-sensitive materials and devices.

Further investigation regarding the ALD growth could be achieved by varying the cycle count, which was set to 300 for all depositions in this work, to verify linear growth or by structural analysis of the grown films, to characterize the interface layer or to asses the films' Hf-O ratio. Depositing layers with different ALD cycle counts and therefore different thicknesses could also help to characterize the asymmetric current-voltage behavior and to verify the relative permittivity ϵ_r determined in this work. Additionally, the specific resistance and the breakdown field may be measured with more precision, by comparing devices with different dielectric thicknesses instead of different capacitive areas.

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A. ALD parameters

The ALD parameters that were kept constant throughout all depositions are listed in Table A.1. The parameters were used on an *AT410* thermal ALD system by *Anric Technologies*.

Table A.1: ALD parameters that are kept constant for all depositions

Parameter	Value	Parameter	Value
ALD cycles	300	DVFill	1000 ms
Purge gas flow rate	34 sccm	DVClose	650 ms
Process chamber pressure	200 mTorr	UFvalve	550 ms
TDMAH exposition	500 ms	Manifold temperature	110 °C
H_2O exposition	500 ms	DV temperature	105 °C
TDMAH temperature	80 °C	Expo on	✓
H_2O temperature	~22 °C	Ozone on	×
TDMAH pulses	2	H_2O & O_3	×
H_2O pulses	2		

B. Device fabrication

Fig. B.1 shows the layout used to fabricate capacitor devices. Green red and blue layers represent the three deposition steps.

Fig. B.1: from top left to bottom right: gold bottom layer (green); HfO_x intermediate layer (red); gold top layer (blue); whole chip design

The following enumeration lists the detailed fabrication steps.

1. **Substrate cleaning**

   The silicon substrate is cleaned in Acetone for 3 min and afterward in Isopropanol for another minute.

2. **Spincoating**

   The sample is spincoated with AZ1505 photoresist for 1 min at 4000 rpm and soft-baked at 100 °C for another minute to remove solvents and partially harden the photoresist.

3. **Photolithography**

   Photolithography was performed on a *Heidelberg Instruments* μMLA system at 10 mW and 30 % power.

4. **Development**

   The photoresist is developed in AZ236MIF developer for 20 s and cleaned for 1 minute in H_2O.

5. **Gold deposition**

   5 nm platinum and 30 nm gold are deposited through sputtering on a *MiniLab 125* magnetron sputtering system by *Moorfield Nanotechnology*, with no rotation.

6. **Lift off**

   The lift off process is started by submerging the sample in N-Methylpyrrolidone (NMP) for at least one hour and completed by manually agitating the solvent over the sample with a pipet, optionally assisted by an ultrasonic cleaner at low power. Afterwards, the sample is again cleaned as in step 1.

7. **2nd and 3rd layers**

   Steps 1 through 6 are repeated for each layer, except that for the 2nd layer, step 5, the deposition of gold, is replaced with HfO_x deposition by atomic layer deposition.

C. Quantization Precision in QAH measurement

Table C.1: Precision of the quantization of R_{xy} and R_{xx} during the gate voltage sweep and magnetic field sweep shown in Fig. 5.3 and Fig. 5.4. The right and left arrows represent the sweep direction with the right arrow corresponding to an increase of gate voltage or magnetic field. $\bar{x}$ shows the mean of both values. Values for R_{xy} and R_{xx} are calculated as the mean in the interval of $-18\,\mathrm{V}$ to $-16\,\mathrm{V}$ (gate sweep), $-2\,\mathrm{T}$ to $0.5\,\mathrm{T}$ (field sweep, increasing) or $-0.5\,\mathrm{T}$ to $2\,\mathrm{T}$ (field sweep, decreasing). The standard deviation of these values provides an estimate of the error.

		Gate sweep			Field Sweep
		$B = -2\,\mathrm{T}$	$B = 0\,\mathrm{T}$	$B = 2\,\mathrm{T}$	$V_g = -17\,\mathrm{V}$
R_{xy}/R_K	$\rightarrow$	0.9924 ± 0.0019	1.0004 ± 0.0026	0.9993 ± 0.0017	0.9944 ± 0.0026
	$\leftarrow$	0.9915 ± 0.0022	0.9990 ± 0.0022	0.9994 ± 0.0019	0.9974 ± 0.0023
	$\bar{x}$	0.992 ± 0.0015	0.9997 ± 0.0017	0.9994 ± 0.0013	0.9959 ± 0.0017
R_{xx} [Ω]	$\rightarrow$	270 ± 40	170 ± 40	240 ± 40	280 ± 170
	$\leftarrow$	280 ± 40	149 ± 28	220 ± 40	220 ± 80
	$\bar{x}$	277 ± 28	158 ± 25	228 ± 26	250 ± 93